JPRS-ESA-84-017

31 May 1984

East Europe Report

SCIENCE & TECHNOLOGY

SELECTIONS ON CSSR COMPUTER TECHNOLOGY

FBIS FOREIGN BROADCAST INFORMATION SERVICE

NOTE

JPRS publications contain information primarily from foreign newspapers, periodicals and books, but also from news agency transmissions and broadcasts. Materials from foreign-language sources are translated; those from English-language sources are transcribed or reprinted, with the original phrasing and other characteristics retained.

Headlines, editorial reports, and material enclosed in brackets [] are supplied by JPRS. Processing indicators such as [Text] or [Excerpt] in the first line of each item, or following the last line of a brief, indicate how the original information was processed. Where no processing indicator is given, the information was summarized or extracted.

Unfamiliar names rendered phonetically or transliterated are enclosed in parentheses. Words or names preceded by a question mark and enclosed in parentheses were not clear in the original but have been supplied as appropriate in context. Other unattributed parenthetical notes within the body of an item originate with the source. Times within items are as given by source.

The contents of this publication in no way represent the policies, views or attitudes of the U.S. Government.

PROCUREMENT OF PUBLICATIONS

JPRS publications may be ordered from the National Technical Information Service, Springfield, Virginia 22161. In ordering, it is recommended that the JPRS number, title, date and author, if applicable, of publication be cited.

Current JPRS publications are announced in Government Reports Announcements issued semi-monthly by the National Technical Information Service, and are listed in the Monthly Catalog of U.S. Government Publications issued by the Superintendent of Documents, U.S. Government Printing Office, Washington, D.C. 20402.

Correspondence pertaining to matters other than procurement may be addressed to Joint Publications Research Service, 1000 North Glebe Road, Arlington, Virginia 22201.

JPRS-ESA-84-017

31 May 1984

EAST EUROPE REPORT

SCIENCE & TECHNOLOGY

CONTENTS

 [III - EE - 65]

CZECHOSLOVAKIA

SELECTIONS ON CSSR COMPUTER TECHNOLOGY

CMOS Technology

Prague SDELOVACI TECHNIKA in Czech No 1, 1983 pp 18-19

[Article by Eng Ladislav Suran and Eng Rostislav Wasyluk, CSc: "Advantages Offered by CMOS Technology in Integrated Circuits"]

[Excerpt] Development of CMOS Technology in the CSSR

In view of the advantages offered by CMOS technology, mainly low power input and a wide range of operational voltages, demands for its introduction in the CSSR appeared in the latter half of the 1970's. Key customers for CMOS circuits are telecommunication technology enterprises for automated electronic private branch exchanges and telephones, enterprises manufacturing communications technology for portable radio stations, and chronometrological enterprises for the production of electronic alarm clocks.

Thus, by the end of 1970 the microelectronics sector of TESLA VUST [Research Institute of Communications Technology of the TESLA enterprise] started developing CMOS circuits with low and medium integration. Since 1980 this development has continued as part of state task AZ 09-119-102 in cooperation with the concern enterprise TESLA Piestany, which is and will remain at the same time the manufacturer of the circuits listed in Table 1.

Circuits of low and medium integration of the 4000 series were supplemented by circuits of high integration on the order of up to 10^4 elements per chip or chip area sizes in excess of 20 mm^2. An outline of the circuits being developed and produced is shown in Table 1. Key properties of CMOS circuits of the 4000 series are listed in Table 2.

Table 1. Outline of Integrated CMOS Circuits Produced or Readied for Production in the CSSR

Circuit type	Designation (nomenclature)
4001	4x2 input gate NOR
4002	pair of 4-input gates NOR
4011	4x2 input gate NAND
4012	pair of 4-input gates NAND
4013	2x flip-flop circuit D
4015	double 4-bit static slide register
4020	14-state binary counter
4024	7-stage counter
4029	two-way linear and decadic counter
4030	4x gates EX-NOR
4046	phase suspension circuit
4029	6x high-capacity invertor gate
4050	6x non-inverting output stage
4051	8-channel analog multiplex
4052	pair of 4-channel analog multiplexes
4053	3x analog twinplexes
4066	4x two-way switch
4068	8-input gate NAND
4076	4x flip-flop circuits D
4081	4x 2-input gates AND
4099	8-bit addressable accumulator
4311	7-segment decoder/exciter with memory
4503	6x busbar exciter
4518	pair of BCD counters
4555	pair of decoders 1 of 4
40114	16x4-bit static memory RAM
1115	integrated circuit for time measuring technology
8804	switching matrix 8x4
5085	integrated circuit for voice frequency dialing (transmitter)
1902A	static memory RAM k x 1 bit
6561	static memory RAM 256 x 4 bits

Table 2. Key Properties of CMOS Circuits of the 4000 Series

(1) Parametr	Symbol	U_{DD} [V]	Min.	Max.
Klidový napájecí proud [μA] (2)	I_{DDO}	5 10 15		0,5 ÷ 50 5 ÷ 100 50 ÷ 300
Výstupní napětí pro L naprázdno [V] (3)	U_{OL}	5 10 15		0,1 0,1 0,1
Výstupní napětí pro H naprázdno [V] (4)	U_{OH}	5 10 15	4,9 9,9 14,5	
Výstupní proud pro L [mA] (5)	I_{OL}	5 10 15	0,5 0,8 3	
Výstupní proud pro H [mA] (6)	I_{OH}	5 10 15	0,25 0,5 2	
Vstupní napětí pro L [V] (7)	U_{SL}	5 10 15		1 2 2,5 ÷ 3
Vstupní napětí pro H [V] (8)	U_{SH}	5 10 15	4 8 12	
Vstupní proud [μA] (9)	I_I	5 10 15		1 1 5

Operational temperature range 0 to 70°C, plastic casings, 14 or 16 outlets. L = log. level 0; H = log. level 1

Key:

(1) Characteristic
(2) Spacing feeder current [μA]
(3) Output voltage for L at no-load [V]
(4) Output voltage for H at no-load [V]
(5) Output voltage for L [mA]
(6) Output current for H [mA]
(7) Input voltage for L [V]
(8) Input voltage for H [V]
(9) Input current [μA]

Most circuits are produced by CMOS technology with Al gates. The introduction of CMOS technology with Si gates is currently underway. It will be used for the production of circuit 4555, memory 6561 and others. Ion implantation and other modern elements of CMOS technology have been incorporated into technological operations. A combination of elements produced by bipolar technology PMOS and CMOS on one chip is represented by, e.g., circuit 5085, voice frequency dailing circuit for pushbutton telephones. Both TESLA VUST and TESLA Piestany plan to introduce the ISO CMOS technology in the course of the Seventh 5-Year Plan.

Conclusion

Circuits made by CMOS technology were as of 1981 becoming part of developmental systems in various enterprises in the CSSR as well. Development in TESLA VUST turned over hundreds of samples of circuits of various types for testing the properties of circuits being developed for specific electronic systems of future devices being developed at more than 40 work centers.

The assortment of circuits of the 4000 series reached in 1982 a total of 19 types of circuits, which will be supplemented in 1983 by six additional types. In addition to the mentioned series, other CMOS circuits including memories--as listed in Table 1--will also become available. It is envisioned to incorporate into development beginning in 1984 additional types of circuits, such as, e.g., CODEC, FILTR, high-capacity memories, etc.

The advantage offered by all the circuit types under development and in production is and will be the fact that they match the catalogue specifications of their equivalents abroad and their useful service life will be guaranteed by the coefficient $\lambda = 2 \cdot 10^{-5}$.

The range of operational temperatures is 0°C to +80°C. As of 1984 individual types of circuits will also be supplied for temperature ranges of -25°C to +85°C, eventually for -35°C to +125°C.

The mentioned assortment of circuits and guaranteed catalogue specifications will enable our enterprises to come up with innovations of electronic systems for digital technology, build systems with minimal consumption of electric energy and high reliability of electronic components.

8080 Emulator

Prague SDELOVACI TECHNIKA in Czech No 3, 1983 p 82

[Article by Eng Frantisek Michalek and Eng Tomas Kolinek: "The 8080 Emulator"]

[Text] Introduction

Despite the various advantages offered by microprocessors, such as an efficient set of instructions, low consumption of energy and low price, there remain areas where microprocessors cannot find application for the time being.

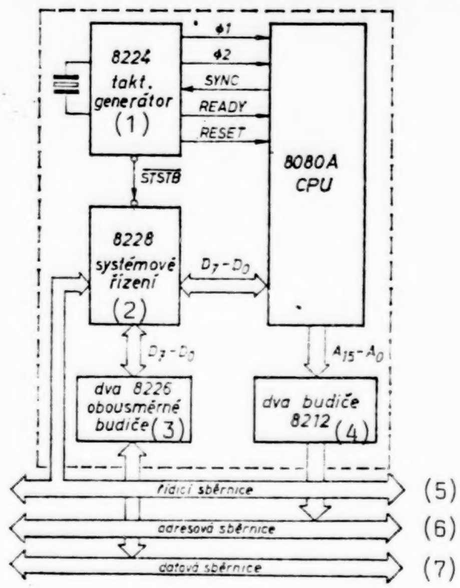
A microprocessor with extensive software is, e.g., the MOS 8080 microprocessor. However, MOS microprocessors are slow and this led to development of the 8080 emulator which considersbly speeds up the system's operation without calling for expensive readjustment of software. Microcomputers of the third generation already have a higher transmissivity than the mentioned emulator.

The 8080 emulator fills in the gap between the usual fast bipolar processors and MOS microprocessors. Even though bipolar processors are adequately fast, they call for requisite development of an assembler and additional software. On the other hand, MOS microprocessors offer assemblers, higher programming languages and developmental systems, but are slow. The 8080 emulator is actually an 8080 microprocessor which operates at a higher speed. In addition to time loops, the 8080 software can be used directly with the 8080 emulator.

Properties of the 8080 emulator:

--complete substitution of seven integrated circuit cases of the 8080A system in accordance with Figure 1;

Figure 1. Complete Substitution of the 8080A System



Key:
(1) Step generator
(2) System control
(3) Two 8226 two-way exciters
(4) Two 8212 exciters
(5) Control busbar
(6) Address busbar
(7) Data busbar

--use is made of microprocessor sections of the MH3000 series;

--it includes a complete set of 8080 microprocessor instruction, also instructions for multiplication and division;

--it includes a free microprogram space for interpretational microprograms for additional instructions;

--instructions are carried out two to nine times faster than with the 8080A;

--the shortest microinstructional cycle, i.e., the time for carrying out a microinstruction, is 150 to 190 ns.

Contrary to the 8080A microprocessor, the length of a microcycle is not limited, a fact that can prove of advantage, e.g., in debugging the emulator or the entire system. The shortest duration of a microinstructional

cycle is determined by the series of TTL circuits used. With the use of a normal series the duration of a microinstructional cycle is 190 ns; with the use of the S series it is 150 ns.

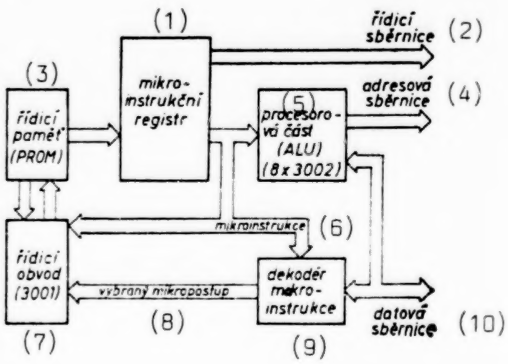
--it offers a choice between a direct or negated address and data busbar.

Wiring Description

The 8080 emulator is built up of bipolar integrated circuits. The emulator's arithmetic unit is formed by eight 2-bit MH3002 sections controlled by the MH3001 microinstructions control unit. The operation of the entire emulator is controlled by a microprogram stored in PROM memories. Instructions in the 8080 are carried out as a series of microinstructions. Microinstructions control directly or indirectly all key blocks of the processor.

A simplified structure of the microprogram processor is shown in Figure 2. It consists of 5 key parts:

Figure 2. Simplified structure of microprogrammable processor



Key:
- (1) Microinstruction register
- (2) Control busbar
- (3) Control memory (PROM)
- (4) Address busbar
- (5) Processor part
- (6) Microinstructions
- (7) Control circuit
- (8) Selected microprocedure
- (9) Microinstruction decoder
- (10) Data busbar

1. Processor part

In it are carried out logic and arithmetic operations, and it is realized by eight MH3002 circuits that form two 8-bit fields. For 16-bit operations both of the fields are interconnected to form 16-bit arithmetic units. Each 8-bit field has a parallel transmission generator. For 16-bit operations there is an additional parallel transmission generator which produces transmission of a 16-bit arithmetic unit.

2. Control Memory

The control memory stores the microprogram. All microinstructions of the emulator have the same format. It is 48 bits divided into control fields. The control memory is formed by 24 74S287-type PROM memories.

3. Microprogram Control Circuit

This part is formed by the MH3001 circuit which controls and generates the sequence of microaddresses for the control memory.

4. Microinstruction Decoder, i.e., emulated instructions of the 8080 series microcomputer

It decodes microinstructions fed from the main memory of the 8080 system. The decoded microinstruction actuates the microprogram control circuit (3001) which generates the initial microaddress of microinstruction in the control memory. Subsequent microaddresses are then determined by the control memory.

5. Microinstruction Register

It serves as a register for carrying out parallel operations. Its function is to retain the microinstruction that is being carried out at the moment and take over a new microinstruction from the control memory during the next microstep.

In the technique of carrying out parallel operations the individual operations, normally carried out in series, are carried out in parallel. This provides for faster carrying out of the operation. The parallel operation technique is applied in two areas in the emulator:

--the single-level technique of parallel operations is used for instantaneous carrying out of a microinstruction and reading a new microinstruction (as one microinstruction is being carried out a subsequent microinstruction is simultaneously searched out in the control memory);

--the multilevel technique of aprallel operations is used in readout of microinstructions from the main memory. During any given microinstructional cycle while the N-th instruction is in progress, instruction (N+1) is readout from the main memory, the address of instruction (N+2) is set up in the internal address register (MH3002) and the program counter is set for the address of instruction (N+3).

Conclusion

The 8080 emulator contains a total of 90 integrated circuits produced domestically or in CEMA countries. The emulator can be positioned on a plate measuring 305x200 mm. The entire emulator uses a single-feed voltage +5 V, current consumption is 5 A. Table 1 shows a comparison of the duration of time needed for carrying out selected instructions of the 8080 emulator and the 8080A microprocessor. Modification of the microprogram makes it possible to add to the set of instructions for the 8080 additional special instructions that could speed up some operations which would have to be carried out by several instructions from the 8080 set. The described wiring of the emulator was implemented by the concern enterprise Zbrojovka in Brno.

Table 1. Comparison of times

1 Instrukce	Emulátor 8080		8080A	
	Počet cyklů 2	Čas μs 3	Počet cyklů 2	Čas μs 3
MOV R_1, R_2	3	0,45	5	2,5
MOV M, R	8	1,20	7	3,5
MOV R, M	6	0,90	7	3,5
MVI R	4	0,60	7	3,5
MVI M	7	1,05	10	5,0
INR R	3	0,45	5	2,5
JMP	6	0,90	10	5,0
$\overline{JMP}$	4	0,60	10	5,0
CALL	13	1,95	17	8,5
$\overline{CALL}$	4	0,60	11	5,5
IN,OUT	8	1,20	10	5,0
PUSH	11	1,65	11	5,5
POP	9	1,35	10	5,0
STA	9	1,35	13	6,5
INX	2	0,30	5	2,5
SHLD	11	1,65	16	8,0

Key: 1 - Instruction
2 - Number of cycles
3 - Time in μs

Caption to Cover Photo

Among the systems and processors SAPI designed for acquisition and processing of information the smallest at the present time is the SAPI 1 shown in our photo of the JPR 1 single-plate microcomputer which on a 150x140 mm plate with printed circuits contains the MHB8080A microprocessor with 8224 and 8228 supporting circuits, memory RAM 1 kilobytes (2 x MHB2114), memory EPROM 1 to 8 kilobytes (1 to 4 x 2708 or 1 to 4 x 2716), input/output circuit with MH3212 and busbar outputs for additional expansion. The JPR 1 microcomputer in simplest applications is capable of independent operation without any supplements. In the interim it can be used also as a substitute until such time as production of our own single-chip microcomputers can be launched. Development of SAPI 1 progressed in the concern enterprise TESLA Elstroj, its producer is the concern enterprise TESLA Liberec and its distributor is the DIZ marketing enterprise of TESLA Eltos. The SAPI 1 system should provide its users with a small system which can find applications in industry, schools, institutions and administration. [Cover photo shows unit with following inscription: K573RF1 OTK 1082 Made in USSR.]

R, L, C, G Measurement

Prague SDELOVACI TECHNIKA in Czech No 5, 1983 pp 161-163

[Article by Eng Karel Kuegler: "New Methods for Measurement of R, L, C, G and Their Applications in Instruments of the TESLA Concern Enterprise in Brno"]

[Text] Demands for automated measurements and digital readout terminated in the course of the last decade the era of bridge methods which up to that time held in the described field a dominant position and were elaborated to a high degree of precision with the passage of time.

However, in their essence they proved unsuitable for continued development toward the automation of metrological processes. Thus, even though they remain unsurpassed in their attained precision, bridge methods have been currently abandoned for application in industrially-produced measuring devices.

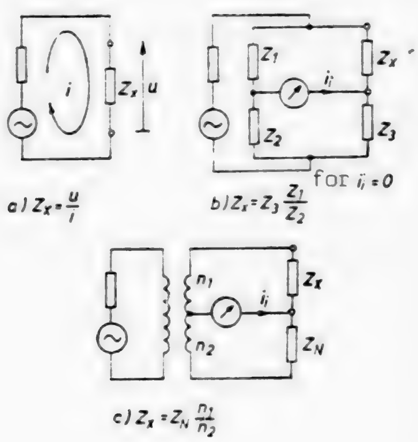
Measuring Methods

Methods in practical use for determining the characteristics R, L, C and G are essentially based on two principles:

a) on using relations of the ohmic law which firmly ties together resistance (impedance), voltage and current and according to which knowing two magnitudes it makes it possible to compute the third one (Figure 1a);

b) on comparing an unknown impedance to an impedance of known magnitude (Figures 1b and 1c).

Figure 1. Basic principles of impedance measurements



Measuring voltages and currents throughout the range of used impedances was no easy matter within the framework of earlier possibilities and thus it was generally more advantageous to use the second method referred to as the bridge or zero method. While in the first method the measuring signal (voltage, current) itself is the carrier of information about the impedance of the measured object Z_x, in the second method it serves merely to indicate the state in which it is possible to read off the values of variable branches of the comparative circuit required for determining the already-mentioned impedance Z_x.

A considerable improvement over bridge methods was the introduction of dividing transformers. Their ratio of division (n_1/n_2) is not subject to external effects and can be arrived at with a higher order of accuracy than normal impedance Z_N. Here the accuracy of measurement is essentially

determined by the precision of a single comparative norm of Z_N. This contingency is put to use in transformer bridges that attain precision of up to 0.01 percent and even higher in the laboratory.

Measuring with instruments using the bridge principle is characterized by a process referred to as bridge aligning, i.e., through gradual approximation toward zero current flow through the diagonal. This, particularly in the case of complex characteristics of the measured object Z_X, need not always be either simple or expedient. Even though automatic balancing of the second component Z_X (as it is used in the latest transformer bridges, e.g., TESLA BM 539) does considerably accelerate the measuring process, there is a need for decisionmaking and for a human operator. It is obvious that the automation of such a process leads to the need to use a servomechanism.

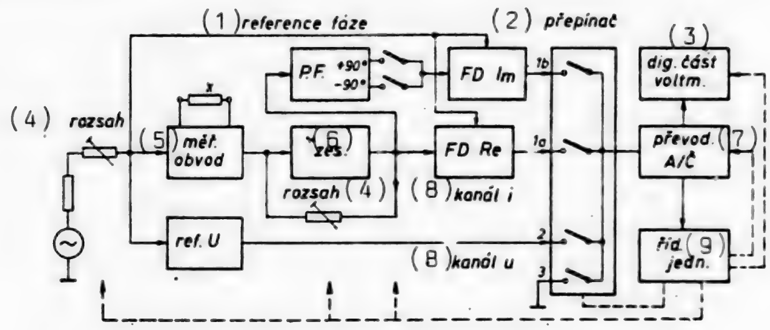
The implementation of the approach mentioned in the previous paragraph is costly and complicated; the useful service life of instruments (automatic bridges) selected for use with the method was not very long. Ultimately, the tie-in to bridge methods was completely abandoned and the basis for numerical measurements is currently constituted by the principle relying on the determination of impedance from measuring voltage and current.

Determination of Impedance From Voltage and Current Measurements

In order to carry out such a measurement, it is necessary to determine the voltage on the measured object Z_X, the current flow through it, and to determine the ratio u/i. As Z_X is generally of a complex character, the current flowing through it has two components: i_{re} and i_{im}. The latter two must be separated by means of a phase-sensitive detector; the real component is in direct dependence on conductivity G, in imaginary dependence on capacity C.

The value of G and C is arrived at by determining the ratio of two magnitudes, i.e., components of current i_{re} and/or i_{im} and the extent of the measuring voltage u_{ref}. Analyzing occurs in the integrator circuit which at the same time converts analog data to digital. The principle of the measuring device's operation is shown in Figure 2.

Figure 2. Impedance meter based on the principle of voltage and current measurements



Key:
(1) Reference phase
(2) Change-over switch
(3) Digital part, voltmeter
(4) Range
(5) Measuring circuit
(6) Amplifier
(7) Analog/digital converter
(8) Channel
(9) Control unit

The measuring circuit is fed a signal from the source of fixed frequency. If an unknown Z_x is connected to the terminals, at its output will appear a signal commensurate to the current passing through. This is amplified in the amplifier from where real components are fed directly into the phase-sensitive detector and imaginary components are fed into the detector via a phase converter. The magnitude of the output signal is adapted to a suitable level by range resistances. The individual rectified voltages are connected by a change-over switch according to the program of the control unit sequentially to the analog/digital converter where the ration of both voltages is transformed into a time inverval. The latter is analyzed in the counter and indicated on the display. Contrary to bridge-type measurement where the configuration of the bridge changes, the measuring circuit for all functions (R, L, C, G, D, Q) remains the same. That is of basic importance in simplifying the design of automated instruments.

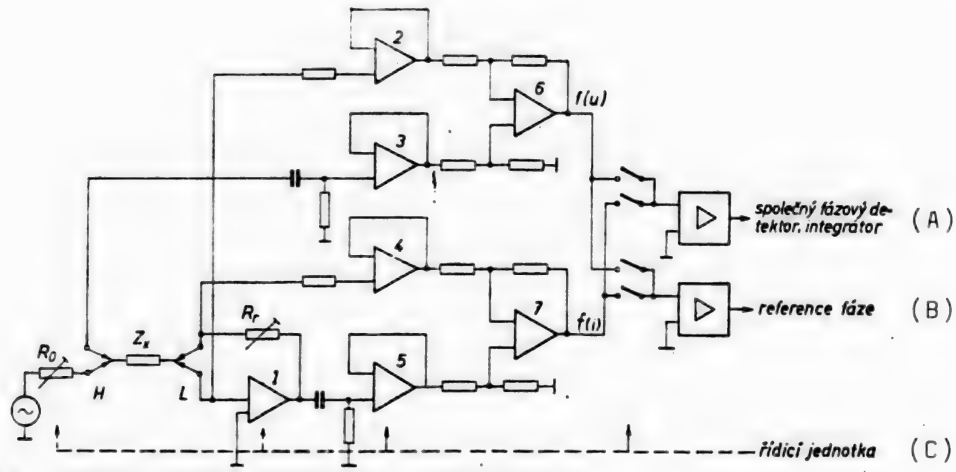
Instrument Wiring

From functional aspects the instrument can be divided into three basic parts.

The Analog Part

This is constituted by a source of the measuring signal, a measuring circuit, amplifiers, rectifiers and change-over switches. Quality functioning of the mentioned part determines in essence the precision of the entire instrument. As such it must be designed with a view to long-term stability; as phase distortion is inadmissible, it calls for active elements with a wide separation between measuring and cut-off frequency. Any error in amplitude or phase is reflected in direct proportion in the precision of measurements. The most demanding circuits include the sensor of voltage and current on the measured object. One of the methods used is shown in Figure 3.

Figure 3. Sensing of voltage and current on the measured object Z_X



Key: (A) Common phase detector, integrator
(B) Reference phase
(C) Control unit

The operational amplifier (1) with resistance Rr in feedback generates at the point of connection of Zx virtual zero, so that object Zx on its L side is very close to the ground potential. The transient current and, thus, voltage on the range resistance Rr are commensurate to the current i flowing through Zx. The voltage is further transformed by means of OZ (4), (5) and (7) into unipolar ground.

Voltage on Zx is detected at the point of its connection and is further processed in OZ (2), (3) and (6). Resistances R_o and R_r change with the range. The purpose of the former is protective and forms at the same time an approximate mode of constant current through the measured object, while the latter modifies amplification.

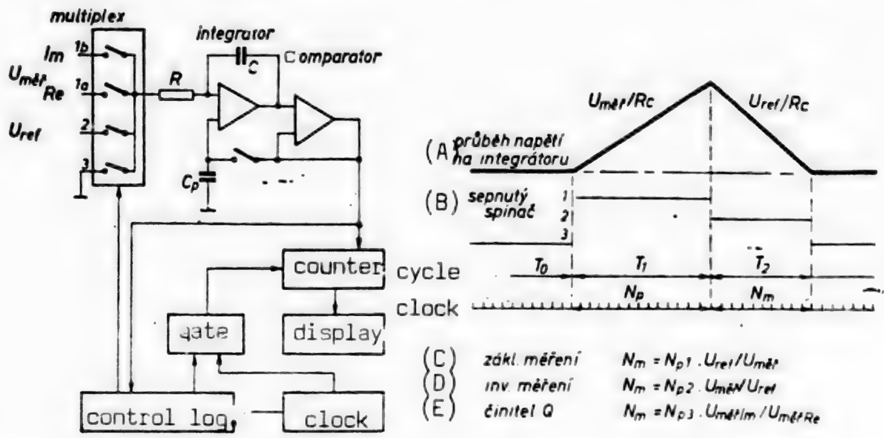
Independent lead-out of terminals and use of four connecting conductors make it possible to eliminate the effects of lead-ins. Both channels (u) and (i) are of identical design to reduce the effect of phase-angle errors.

As the measured factor (R, L, C, G) is arrived at from the ratio of two components, use of a common channel makes it possible in part to eliminate the effect of drifts along this entire path. In this case (contrary to Figure 2) the change-over switches are located directly behind the sensors, as can be seen in Figure 3, and the subsequent path is shared in common alternately for current i and voltage u. This particular method calls for a special rectifier which smoothes out the rectified voltage in the course of a few cycles of the measuring frequency.

Analog/Digital Converter

The "double integration" method is used in digital measurement of voltage for conversion of analog data to digital. In our case it is used additionally for direct analysis of the impedance components (R, L, C, G). The functioning of such an analog/digital converter operating in three cycles is indicated in Figure 4.

Figure 4. The "dual slope integration" method as the basis of an analog/digital converter for assessment of impedance



Key:
(A) Voltage distribution on integrator
(B) Actuated change-over switch
(C) Basic measurement
(D) Inv. measurement
(E) Factor Q

In the initial state the control unit actuates connection of voltage U_{mer} (1a or 1b) to the integrator and start-up of the counter. When the latter counts off the programmed number of pulses N_p it is switched to the integrator U_{ref} (2), the counter starts counting again unless it is instructed to stop while going through zero. The count of N_m pulses depends on voltage U_{mer} and is numerically indicated. In the third zeroing act, zero drift is eliminated by means of the memory condenser C_p.

Let us assume that the measuring circuit in accordance with Figure 2 yields an output voltage commensurate to the parallel combination of G and C. Then during connection of switch (1a) there occurs measurement of conductivity G, and during connection of switch (1b) capacity C is measured. Assessment of G in inverse form, i.e., resistance R, is achieved simply by switching the dequence of fed-in voltages U_{mer} and U_{ref} into the integrator. Similarly, it is possible to assess inductivity as $L = -1/w^2C$. If the integrator is fed voltage (1a) in cycle T_1 and (1b) in cycle T_2, then the number of clock pulses N_m is commensurate to the loss factor D and, conversely, the quality factor Q.

Control Unit

This is the functionally most complicated part of the instrument. In it are concentrated all control functions of the instrument. It controls the functioning of the converter, the digital part of the voltmeter, indication of dimensions and decimal points and carries out automatic range selection. Control logic in the case of simpler instruments takes the form of a diode matrix, logical circuits.

Application of a microprocessor in this part facilitates considerable expansion of the potential for measurements. This can be, e.g., determination of deviation in the dimensions of a given factor or percentage deviation from nominal values, improved precision and read-off through determining an average from a greater number of measurements, computation of derived parameters, use of a greater number of measuring frequencies and levels of measuring signals, automatic correction of errors caused by connecting cables and residual parameters of the instrument, etc.

Instruments controlled by a microprocessor do not use analog/digital converters for analyzing the measured quantities, but determine them directly by calculation from the magnitudes of the four components of vectors of voltage and current.

Comparison of Instruments Based on Either Principle

From the viewpoint of the user the key contribution is provided primarily by those properties that generally characterize all digital instruments. They are expediency and ease of measurement, reduced dimensions and weight of the instrument, possibility for its integration into the measuring system. This calls at the present time for paying an approximately three times the price of an instrument based on the bridge concept and offering comparable precision of measurements.

Instruments based on the u/i principle of measurement cannot match the former transformer bridges in precision. In the latter, high precision and long-term stability was based on a single normative standard designed for that purpose. In new instruments the parameters are determined by several dozen precision resistances and semiconductors used in the instrument along the signal path from the measuring terminals all the way to the integrator. That constitutes the main reason why the new measuring devices currently achieve a maximum precision of 0.1 percent, to a limited extent top precision of 0.05 percent.

If we use an instrument for measurements, an advantage is offered in the absolute majority of cases by the unambiguous nature of a digital readout. An exception is formed by repeat measurements of components (tolerances) where analog indication of the measuring device is preferable as it requires considerably less attention on the part of the operator.

RLCG Meters From the TESLA Concern Enterprise in Brno

The last transformer bridge and predecessor of a new generation of measuring devices is the semiautomatic instrument BM 539. It uses automatic compensation of the second component, offers a possibility for tolerance measurements with basic precision of 0.05 percent. In cooperation with the BP 5390 sorter it automatically sorts components with axial taps.

The u/i measuring principle is used by the RLCG bridge-voltmeter BM 559. Its hybrid measuring circuit (with partial use of transformers) facilitates measurements in a wide range of 13 decades. The device can also be used as a 2-channel voltmeter. The digital readout is read off on two 4 1/2-digit displays, basic precision for measuring components of impedances and voltage is 0.1 percent. Incorporation into the system permits the use of a built-in circuit for the IMS-2 contact. The instrument uses the 2-channel system shown in Figures 2 and 4.

The BM 591 meter with basic precision of 0.25 percent is designed for the widest range of applications. It uses digital readout of R, L, C, G, and D on a 3 1/2-digit display, automatic range selection, two measuring frequencies (1 kHz, 100 Hz) and two levels of measuring voltage (1 V, 50 mV). Its low measuring frequency (100 Hz) makes it suitable for measuring high capacities and inductances, its low level of the measuring signal (50 mV) facilitates measurement of the properties of semiconductors. The device uses the measuring circuit wiring shown in Figure 3 with a common channel for both analyzed magnitudes i and u.

Figure 5. The BM 539 semiautomatic transformer bridge offering basic precision of 0.05 percent

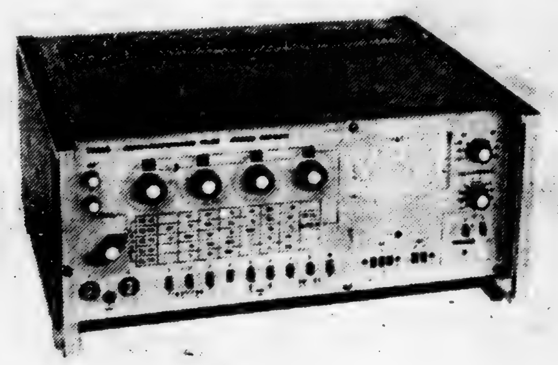
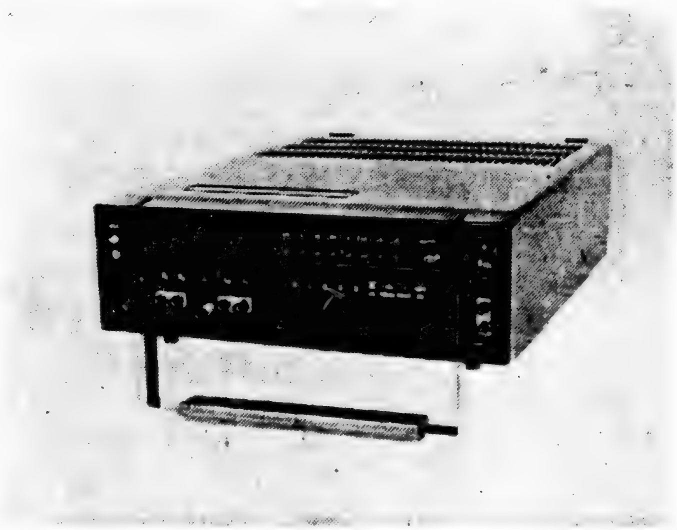


Figure 6. The BM 559 automatic digital bridge-voltmeter offering basic precision of 0.1 percent

Figure 7. The BM 591 automatic digital meter with automatic range selection offering basic precision of 0.25 percent



Quality Analysis

Prague SDELOVACI TECHNIKA in Czech No 11, 1983 pp 401-402

[Article by Eng Pavel Kyjovsky: "Quality Analysis in the Concern Enterprise TESLA Kolin"]

[Text] Quality analysis and quality engineering are one of the means for intensifying the national economy that have an impact not only on the sphere of products, but also on the management and evaluation of entire production organisms in defining their economic and social utility. Quality analysis as such is a system-oriented complex of methods, the ultimate objective of which is searching for and proposing improved or even basically new solutions relevant to the function of the analyzed object in order to improve its effectiveness.

The following are characteristic of the substance and principle of quality analysis:

a) The object, for which the method is used, is interpreted and described as a set of functions.

b) The briefly described functions are assessed from the viewpoint of their significance, costs and the degree of meeting their purpose.

c) The criterion of the solution's effectiveness is the relation between the level of meeting a social need expressed in the degree to which the function has been met and the costs of its implementation, formulating thus an indicator of its relative effective value.

d) The sequence of stages, steps and operations is adhered to in quality analysis as a verified methodological procedure.

e) Methodology of quality analysis calls for an interdisciplinary approach--that takes mostly the form of teamwork--to dealing with a problem.

The most frequent use of quality analysis as an efficiency-promotion method is encountered in the area of product innovations in almost all the branches of the national economy, but it can also be effectively applied to the generation of new objects, i.e., in research, development, technical preparation of production as well as planning of investments, and is a suitable instrument for dealing with such problems as finding new and more efficient ways of utilizing by-products and waste or scrap.

The objective of the quality analysis experiment--conducted by the CSVTS [Czechoslovak Scientific and Technical Society] Central Section of Specialists in Quality Engineering of the Czech Central Council of the Committee for Scientific Management in cooperation with the Government Council for Dealing With Problems of Planned Management of the National Economy--is to create conditions for the widest possible application of

quality analysis and of quality engineering as effective tools for intensifying the national economy. The quality analysis experiment is oriented toward the sphere of price setting, plan indicators, individual incentive systems and state goal-oriented programs.

The quality analysis department was established in the concern enterprise TESLA Kolin on orders of the enterprise manager as of 1 January 1974 and, thus, the specified year became a trial year. In the subsequent year was determined the limit of savings which the quality analysis department had to achieve in order to preclude cutbacks in the amount of the premium allocated to its personnel. The quality analysis program in TESLA Kolin was divided into three groups formed by the sector of telecommunications and, within it, the DVK and DVS translators for automation of our long-distance telephone network, the sector of aviation radio engineering with small radio stations and automatic direction finders carried aboard aircraft and the sector of numerical control systems that includes systems of the third generation, programmable automated devices and systems for computerized numerical control (CNC) with microprocessors.

Classified as completed tasks are those solutions submitted by teams whose proposals had been approved by the relevant department, passed review proceedings and had the term for their implementation set. Other tasks do not qualify for inclusion in the savings limit. The amount of savings is determined for turned-out production by economic analysis and depends on the contributions derived from the new design, finish or workmanship and the number of units produced in 1 year following the date of approval of the change. Savings in the area of overhead expenses are determined individually depending on the nature of the completed task.

The best justification for the method of quality analysis in the electrotechnical and electronic industry is provided by the results achieved through the application of quality analysis. The savings attained in individual years in thousands of Kcs were as follows: 1975--205, 1976--246, 1977--291, 1978--186, 1979--233, 1980--360, 1981--304, 1982--144. From this outline it is obvious that application of quality analysis produced in the initial period alone savings exceeding the amount of Kcs 1.6 million, through noninvestment means, suitable for characterizing as small-scale efficiency promotion measures.

Let us now cite several examples of products to which the quality analysis method was applied.

The 5FA 494 22 soldering tip for DVK and DVS translators used to be made from a brass rod of 2.5 mm diameter which was turned by lathe and provided with silver-coated surface finishing. In current use is a brass wire of 1.6 mm diameter which is cut by machine into 12.7 mm lengths and is pressed on the copper foil side into a plate with a printed circuit. After pressing in the tip ends are coated with soldering varnish and 15 tips are pressed simultaneously by the CDC-2 hydraulic press. With a saving of Kcs 0.075 per unit, the annual savings amount to Kcs 148,337.

Parts of S and LV stands used to receive their surface finish by coating with copper and nickel in accordance with the technological procedure NT 1501. After testing it was proposed to provide surface finishing for parts 5XA 62230 and 86545 by zinc and chromium coating, it being functionally equivalent to the original finishing at lower overhead costs. The original concept translated into Kcs 0.57 per square decimeter; the new concept translates into Kcs 0.16 per decimeter square and annual savings amount to Kcs 145,332.

In the case of DVK and DVS translators of layout drawing numbers 5FP 554 16 through 23, 26 and 27 the plates were connected with the body of the translator batten by means of conventional connecting parts--angle irons, screws, washers and rivets. These were replaced by prestressed flexible flanges that are riveted directly to the translator's batten, which also provided the possibility for tipping the plates out for installation and repair. This solution represents considerable savings of labor-intensive efforts taken up by the eliminated connecting parts. With approximately 11,000 translator units, the savings of labor and materials amount to Kcs 148,961.

Quality analysis of product NS 910 was used to provide specifications for the 5XN 670 00 input transformer, the original design of which consisted in attaching a ferrite core with a coil into a plastic casing consisting of two parts in which were imbedded four outlets for soldering on the coil outlets. The soldering referred to was considerably labor-intensive and the transformer was attached to the plate with printed circuits to the already-mentioned four outlets by manual soldering. The new concept consists in attaching the ferrite core with coil directly to the printed circuit by means of a simple metal fastener. Outlets from the coil are reinforced by twisting together, which makes it possible to use wave soldering even in their case. This concept brought about savings in labor-intensity and partially even in materials.

Casing for the IME 2VN scanner used to be produced from three parts connected by capillary soldering, i.e., this technology represented a considerable volume of labor-intensive operations for each individual part as well as for the entire set. After the performance of quality analysis it was proposed to use a similar part from the Industrial Automation Plants in Kosire, where it is drawn from sheet metal in one piece. This eliminated the need for machine cutting and capillary soldering. With annual production of 1,850 units, the savings represent 3,542 standard hours that amount to Kcs 138,380.

In the case of the 5FK 282 06 socket, its body was made of two units and its contact spring consisted of three pieces held by the upper part of the socket. The position of the two parts of the body had to be mutually secured prior to assembly by tying them over with wire which during assembly again had to be removed. The new concept consists in designing the socket body and the contact spring from a single piece, and the position of the spring is adjusted by slightly turning its bottom part. This does away with labor-intensive operations in assembling the spring and

mutual positioning of the two parts of the socket's body prior to assembly. The savings in materials are Kcs 97,790, in standard hours 12,261, which represents total savings of Kcs 322,650.

Switch blades used to be fastened in the body of the 5FF 897 21 connecting plug by means of two pins, and making openings in the body of the plug was considerably labor-intensive and resulted in a high rate of rejects. The switch blade consisted of three parts and its assembly was considerably labor-intensive. The proposed solution is based on pressing the contact spring and the switch blade as a single part by means of the ALO 20 automated press. Slots are provided in the body of the plug in the switch blade and in the pressed out portion of the plug's body. The concept generated material savings in the amount of Kcs 65,018 and savings of 10,965 standard hours, for a total savings of Kcs 304,150.

The 5QA 548 12 through 14 and 5QA 548 16 through 19 segments used to be gold plated on both sides, but the sensing contact registered only a part of the gold-plated area. The proposed solution consisted in covering the nonfunctional areas of the segment with acrylate varnish and gold plating only the remaining area of the segment where the segment and the contact meet. The computed saving of material (potassium dicyanoaurate) arrived at through economic analysis represents an amount of Kcs 60,000.

After having gained favorable experience with the application of quality analysis and after verification of its methodology in the preceding years, TESLA Kolin is starting in the current year to apply it to more complicated production units and additional parts. Among the latter is a second variant of economic gold plating of the 5QA 54812, 13 and 21 segments. In the cases of the latter, detailed specifications were provided as to which spot is to be gold plated (inner or outer). This provides additional savings of potassium dicyanoaurate.

Another task in the application of quality analysis to devise a new concept for output terminal connectors for high-performance switches. The existing terminal connector consists of two parts. The task of quality analysis in this case is to devise the formation of each terminal connector as a unit by means of the ALO press. This will reduce (in view of the annually produced amount of approximately 80,000 terminal connectors) the demand on capacity in preproduction stages. In addition to the already-mentioned tasks in the application of quality analysis to parts, the quality analysis group will form a team for devising methdology for the redesign of a complete product.

Soviet Television Sets

Prague SDELOVACI TECHNIKA in Czech No 11, 1983 pp 405-406

[Article by Eng Pavel Votava: "Soviet Television Receivers of 1983"]

[Text] According to the last 5-year plan the Soviet electronic industry increases every year the number of VTV [color television] receivers it

produces. For example, in the third year of the 5-year plan the production program of individual Soviet enterprises will include around 50 types of receivers with diagonal screen measurements of 67, 61, 51, 32 and 25 cm and roughly 20 types of black-and-white TV receivers with diagonal screen measurements of 61, 50, 40, 31 and 23 cm.

Among the most produced in the Soviet Union since 1980 were second class BTV receivers with a diagonal screen size of 61 cm. These were unified hybrid receivers, types using integrated circuits and modular receivers designed exclusively with the use of semiconductor elements and integrated circuits. Also in production were portable fourth class BTV receivers with diagonal screen size of 32 and 25 cm, the production of which is to be continued.

The above-mentioned types will be supplemented in 1983 by unified modular BTV receivers with semiconductor elements, IO [integrated circuits] and diagonal screen size of 67 cm of the second quality class--Rubin C-230 (Figure 2) and Elektron C-265D, and unified types with diagonal screen size 61 cm of second class--Vityaz C-220 and C-22, Gorizont C-255 and Elektron C-275 and C-280.

Production started on BTV receivers second class on a unified chassis with diagonal screen size 67 cm type Elektron C-260 (Figure 3), additional unified types based on semiconductor elements and IO third class (diagonal screen size 51 cm), Rekord VC-311. In stores there appeared new types of unified portable BTV receivers designed by means of semiconductor elements and integrated circuits included in the fourth quality class with diagonal screen sizes of 32 cm--Shilyalis C-410 and Yunost C-404, and 25 cm--Shilyalis C-420.

Table 1 shows the basic technical specifications for BTV receivers manufactured by the Soviet electronics industry in 1983. Receivers with diagonal screen size of 67 cm (types Rubin C-230, Elektron C-260D and Elektron C-265D) use input parts for meter and decimeter wave bands (TV band I through IV), sensor-type control elements with luminous indication of the number of the selected channel. The receiver type holding the greatest promise for the future is Elektron C-265D which at low weight (38 kg) uses a substantially lower power input in comparison with hybrid types of television sets (80 W).

Figure 1. View of several portable black-and-white and color television sets of Soviet manufacture

Figure 2. Color television receiver type Rubin C-230

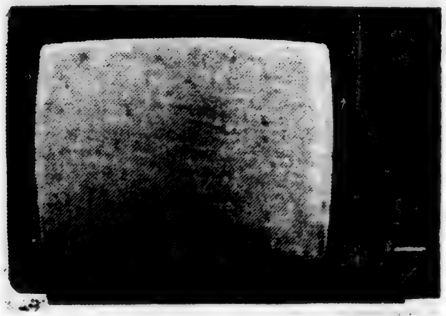


Figure 3. Color television receiver type Elektron C-260

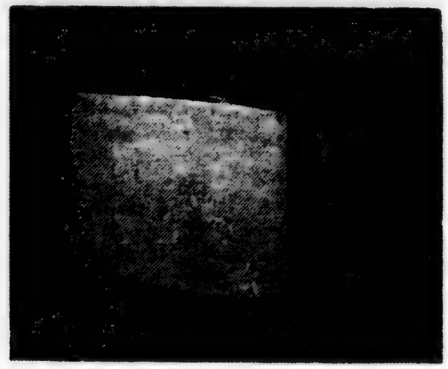


Table 1. Basic technical data of BTV receivers produced in the USSR in 1983

1 Typ televizoru	2 Úhlopříčka [cm]	3 Pásmo	4 Citlivost (µV)	5 Výstupní výkon zvuk [W]	6 Příkon [W]	7 Rozměry [mm]	8 Hmotnost [kg]	9 Přepínač kanálů	10 Cena [Rbl.]
Rubin C-230	67	m/dm	55/90	2,5	185	790 × 510 × 470	54	S	1300
Elektron C-260D	67	m/dm	50/90	2,5	120	780 × 520 × 460	38,5	S	1300
Elektron C-265D	67	m/dm	55/90	2,5	80	786 × 528 × 455	38	S	1300
Horizont C-255	61	m	55	2,5	120	745 × 496 × 550	37	S	850
Elektron C-275, 280	61	m	55	2,5	100	795 × 492 × 544	36	S	850
Kvarc C-202	61	m/dm	80/300	2,5	190	750 × 530 × 550	50	S	790
Temp C-203, 207, 208	61	m/dm	80/150	2.5	185—200	750 × 520 × 550	50	S	790
Rubín C-205	61	m/dm	55/90	2,5	185	750 × 550 × 520	50	S	850
Vitjaz C-220, 222	61	m	80	2,5	150	790 × 530 × 530	45	S	775
Sadko C-220	61	m	55	2,3	180	750 × 520 × 555	45	S	796
Foton C-220	61	m	50	2,5	150	750 × 495 × 555	40	T	755
Elektron 716									
Rekord 726									
Jantar 726	61	m	50	2.5	250	800 × 550 × 550	60	K	860
Lazur 722									
Sadko 722	61	m/dm	80/300	2.5	250	744 × 530 × 565	60	S	755
Vitjaz 733, Sadko 733, Spektr 733, Temp 733, Raduga 734, Horizont 736, Rekord 736									
Foton 736, Tauras 736, Jantar 736, Lazur 738, Čajka 738, Temp 738, Elektron 738									
	61	m	55	2.5	250	780 × 560 × 516	60	S	720
Rekord VC-311	51	m	100	1.5	120	640 × 450 × 470	30	T	690
Šiljalis C-410	32	m dm	100/140	0,7	75	430 × 305 × 325	13	T	498
Junosť C-404	32	m	100	0,75	90	460 × 342 × 350	16	S	520
Šiljalis C-420/I	25	m/dm	100/140	0,25	55	370 × 240 × 270	8,7	S	478

Channel selectors: S - sensor-type; T - push-button type; K - revolving

Key:

1. Type of television set
2. Diagonal screen size in cm
3. Band
4. Sensitivity in microvolts
5. Audio output in watts
6. Power input in watts
7. Dimensions in mm
8. Weight in kg
9. Channel selector
10. Price in rubles

Viable types also include models of receivers with diagonal screen size of 61 cm--Gorizont C-255 (Figures 4 and 5), Elektron C-275 and C-280 that also underwent a considerable reduction in weight and power consumption. Their unified design (forming an integrated unit) makes their servicing easier. They use sensor-type program control with luminous indication of channel numbers.

The type Gorizont C-255 uses many monolithic and hybrid integrated circuits, sensor-type control of input channels and guarantees quality reception of color and black-and-white TV signal in the I through III TV bands according to OIRT recommendations. Supplementing it by the SK-D-24 functional block facilitates reception of television programs in the IV and V TV band, including infrared remote control.

Figure 4. Color Television receiver type Gorizont C-255

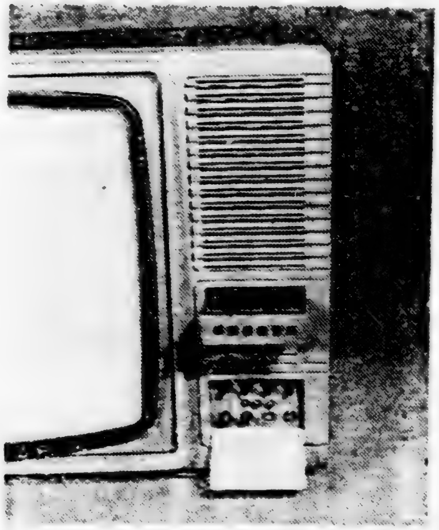


Figure 5. Color television receiver Gorizont C-255--close-up of controls

The Gorizont C-255 belongs to the so-called new generation of BTV receivers. It offers a number of advantages over the currently produced types in that it uses new electronic parts technology: the processing of TV signals provides improved quality of television image (higher chromatic purity and improved definition of image sharpness), higher sensitivity and automatic gain control, and improved reliability is achieved by reduced operational temperature within the TV set housing by a substantial cutback in the set's power input. The weight of the Gorizont C-255 receiver was reduced by half (36 kg); its dimensions are length 495 mm, width 745 mm and depth only 550 mm. The receiver is also offered with a variant of the SDU-3 type wireless remote control variant which makes it possible to operate the TV set from a distance of up to 8 meters. It uses the SK-M-24-1 type input part (channel selector). The Gorizont C-255 BTV receiver is shown in Figure 4 and was exhibited by the foreign trade enterprise Tekhnointorg at the International Exposition of Socialist Countries in Brno in 1983.

The Elektron C-275 and C-280 types come equipped with digital clocks which can automatically turn the set on and off according to the preset times. Modular types of this category use either sensor type or push-button control elements for channel selection together with channel number indication. During repairs they can be hooked up to diagnostic devices for expedient identification of defective modules. Their weight and power consumption is also lower than that of hybrid types.

Television sets Temp C-203, C-207 and C-208 are modifications of the type Temp C-202. The C-207 type offers optional audio accompaniment transmission in the infrared region into a special headset. Wireless remote controls can be connected to the C-208 type. The Rubin C-205 offers in addition a built-in block of video games.

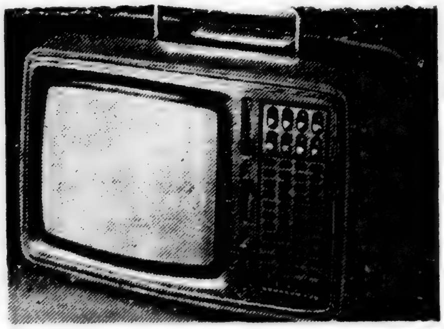
In comparison with the preceding generation, it became possible substantially to reduce the power consumption and weight of modern BTV receivers with semiconductors and diagonal screen size of 61 cm (using modern power supply sources). Remaining in production--in addition to BTV receivers with a 61 cm diagonal screen size--are the popular hybrid television sets Lazur-714, Rubin-714, Rekord-714, Chayka-714, Raduga-716, Raduga-719, Chayka-722 and Elektron-736. These are described in greater detail in reference [2]. New models of the mentioned subgroup are listed in Table 1.

In the case of the new BTV receivers with a 61 cm screen it is possible to supplement the input part of the decimeter band (TV band IV and V). Models with this part already built in show in their type designation the supplementary letter D and their price is higher by 35 rubles than without it. Production of hybrid BTV receivers with a 61 cm screen which still account for a great volume of production will be gradually reduced and discontinued in 1985.

A new BTV receiver with a 51-cm screen, the type Rekord VC-311, is also slated to make its appearance in stores in 1983. It is envisioned that it will become the most widely used television set in the USSR. It uses a push-button channel selector with luminous channel indication, modular design and transformerless power supply.

New models of portable BTV receivers with diagonal screen size of 32 cm are represented by the types Shilyalis C-410 and Yunost-404. Due to transformerless design of the power supply source in the type Shilyalis C-410, its weight could be reduced to 13 kg and its power input cut back to 75W; it uses a push-button channel selector and a modular block design. The Yunost C-404 uses a sensor-type channel selector, its weight is 16 kg, power input 90 W. Production of the popular types Shilyalis C-401 (Figure 1) and Elektronika C-401 will continue. Ready among BTV receivers with a 25-cm screen is the new type Shilyalis C-420D, and production of the type Elektronika C-430, known also in our country, will continue (Figure 6).

Figure 6. Portable color television receiver Elektronika C-430



Only a few changes occurred in the assortment of black-and-white television receivers since 1980. The new models listed in Table 2 show almost no difference in their technical specifications from those described in reference [2]. The new types in the area of black-and-white television sets are Yunost-405D (31 cm), Safir-402 (23 cm), Elektronika-450 (11 cm). The television sets Yunost-405 and Safir-402 use a push-button channel selector.

Table 2. Basic technical data for black-and-white TV receivers produced in the USSR in 1983

1 Typ televizoru	2 Úhlopříčka [cm]	3 Pásmo	4 Citlivost [µV]	5 Výstupní výkon zvuk [W]	6 Příkon [W]	7 Rozměry [mm]	8 Hmotnost [kg]	9 Přepínač	10 Cena [Rbl.]
Slavutič 219	61	m	50	2,0	180	700 × 550 × 430	42	K	290
Tiuras 211	61	m	50	2,5	180	720 × 490 × 420	35	K	296
Rekord 345	50	m	110	0,5	160	600 × 450 × 360	28	K	200
Jantar 312	50	m	110	0,5	155	515 × 505 × 375	27	K	206
Junosť 405D	31	m/dm	30/100	0,75	33/17*	392 × 305 × 290	9	T	295
Safír 402	23	m	30	0,3	25/17*	325 × 225 × 225	6,5	T	220
Elektronika 450	11	m	100	0,05	10/6*	190 × 150 × 90	2,2	K	140

Channel selectors: T - push-button type; K - revolving; * - power supply network/battery

Key:

1. Type of television set
2. Diagonal screen size in cm
3. Band
4. Sensitivity in microvolts
5. Audio output in watts
6. Power input in watts
7. Dimensions in mm
8. Weight in kg
9. Channel selector
10. Price in rubles

BIBLIOGRAPHY

1. Borobkov, N., "Television Sets 83," RADIO No 1, 1983, pp 25-27.

2. Slepnyeva, V., "Television Sets 80," RADIO No 1, 1980, pp 24-26.

3. Votava, P., "Development of Soviet Consumer Electronics," SDELOVACI TECHNIKA No 1, 1983, pp 401-403.

Robots, Manipulators

Prague SDELOVACI TECHNIKA in Czech No 12, 1983 pp 441-442

[Editorial by Eng J. Grecner: "Robots and Manipulators in the Sector of the Federal Ministry of the Electrotechnical Industry"]

[Text] An extensive series of technical and popular articles and addresses dealing with the problems relevant to industrial robots and manipulators (PRaM) leaves by its contents in nobody's mind any doubt that the agenda of the day includes a substantial modernization of the productive base

of the Czechoslovak industry. The significant share of organizations of our sector in the state goal-oriented program--be it the technological development of PRaM, development of their production or the area of their application--can be judged from the following data.

On the part of the sector of the FMEP [Federal Ministry of Electrotechnical Industry], the key place in technological development of PRaM is held--due to their significance--by the concern ZAVT [Automation and Computer Technology Enterprises] Prague and the VUVT [Research Institute of Computer Technology], Zilina which is developing--as part of a task of the state plan for technological development--a new 16-bit microcomputer for a PRaM control system. Relatively high technical demands on the quality of the control system, mainly with regard to speed and reliability, were made on the part of VUKOV [Research Institute of the Metallurgical Industry] Presov, the project's coordinator and cooperating organization. It was decided to adopt a modular concept design permitting a high degree of variability in the composition of the control system while meeting the basic prerequisite for developing effective international cooperation and specialization among relevant organizations in interested CEMA countries. The task solvers have recently started generating applicational software, which is being developed with adequate time lead. Another part of the task will be the development of a microprogram-controlled connecting unit for connecting several sensor-type subsystems and sensors typical of the new generation of adaptive PRaM. The technical orientation of PRaM, involving many management and decisionmaking processes in real time, will even call for a multilevel and multiprocessor concept in dealing with software and hardware. The control system uses exclusively microcomputers of the uniform series SMEP [System of Small Electronic Computers] (product of the ZVT [Computer Technology Enterprise] Banska Bystrica), with the subsequent production of the PRaM control systems being provided by the ZPA [Industrial Automation Enterprises] DUKLA Presov.

A completely independent and goal-oriented approach to the development and production of PRaM was selected by the ZSE [High-Voltage Engineering Electrotechnical Enterprises] concern Prague. As early as 1977 the VUSE [Research Institute of High-Voltage Engineering] Bechovice launched developmental efforts involving PRaM with unconventional application of asynchronous three-phase motors for providing electric power drives while systematically adhering to the principle of using the domestic base of spare parts. An original functional concept of the control system that meets not only the predetermined algorithms of PRaM control in automated operation, but also its synchronization with the technological system, made it possible to achieve relatively high technological specifications (e.g., positioning better than ± 5 mm) adequate for some workshops engaged in mechanical processing. Success was also encountered in the application of electric drive to PRaM gripping heads (instead of the still-used electromagnets) and in the development of harmonic reducers of revolutions of electric drives for PRaM.

The FMEP sector's tasks relevant to production are implemented by three organizations: the ZAVT concern in the concern enterprise DUKLA Presov, which is taking over and implementing the developmental results attained by VUKOV Presov with the so-called type series of PRaM; and the ZSE Prague concern which is preparing construction of new capacities in the Horice plant of the ZEZ [Thermoelectric Systems Enterprises] Prague concern enterprise to meet the demanding tasks it faces in PRaM production. Specific direction for the application of PRaM in the electrotechnical sector, where typically machine-building production is not extensive and where there prevails production and assembly of small-dimensioned electronic and electrotechnical instrumentation and systems, PRaM application will be called for in flexible assembly systems and lines, the development--and partially also production--of which is provided for by VUMA [Research Institute of Mechanization and Automation] Nove Mesto on the Vah River. Also particularly desirable is the widest possible individual application of technological units from the mentioned systems, because with minimal demands on foreign exchange as well as ease of installation and programming they offer great possibilities for promoting efficiency and automating individual production operations. Initiative is developed in this respect by the concerns TESLA-Consumer Electronics and Chirana.

After successful mastering of many PRaM applications in industrial production there is setting in the demanding period of improving their quality and reliability. If we take into consideration the fact that the average time between the development of defects by individual PRaM turned out by their world's leading producers amounts to only several hundred hours, we must necessarily admit that it is specifically qualitative standards that are the limiting factors in the contemplated projects for the mass application of PRaM. The state goal-oriented program 07--within which PRaM development in the CSSR is dealt with--therefore sets of goal of achieving in domestically produced PRaM up to 600 hours of average time between the development of defects. The coefficient of technical utilization of PRaM (expressing the effectiveness of their application) is to increase in this manner to an anticipated value of 0.95 to 0.98. An additional conspicuous increase in the reliability of PRaM is expected after 1985 in connection with innovations in the electronic and electrotechnical spare parts base. The current--and not very satisfactory--state can be characterized by the adage which holds that the strength of a chain is determined by its weakest link. Preliminary analyses indicate a considerable imbalance in the quality of parts that make up the serially connected system and parts that degrade the system's reliability, and operational reliability was found to be one order below its theoretical equivalent. Thus, the inherent and operational reliability of the control system produced by organizations of the FMEP is becoming the center of attention among interested developmental and design/production units as well as parts manufacturers. However, in the order of urgency for dealing with the most acute problems of reliability, the first place is no longer held by the electronic part of the system, but mainly by electromechanical elements (e.g., circuit breakers, contactors, switches) and also by oproelectric elements, switches controlled by magnetic field and some

peripheral devices. Thus, the weakest links of the chain are gradually being discovered. The credibility of reliability computations, eloquence of assessments and analyses as well as the simple fact of the not quite satisfactory reliability of PRaM used in industrial production are all reasons for all acquired data to become the basis for the orientation of future tasks in the area of technological and investment development.

It is obvious that viewpoints of economic effectiveness of PRaM application, the rate of return on investments and the methodology for assessing their contributions had been underestimated in the initial period and are often referred to as obstacles to PRaM development. However, a partial redress has already been achieved. However, specialization of design and planning components will be more difficult to come by and will not progress quite as rapidly. The crux of the problem is constituted by the fact that it is not until after the completion of design and planning studies--which in the case of automated technological work centers (ATP) can take up to a year--that a decision can be made as to what types of PRaM are suitable for a given task, and there is also the need for logistical backup. All this considerably prolongs the time between intent and implementation. Nevertheless, accelerated construction of design and planning capacities is under way, and their specialization, e.g., in Elektroprojekt Prague, should provide a guarantee for the successful introduction of PRaM and mainly of ATP in the coming period.

Under conditions of the FMEP sector the most topical task is the application of goal-oriented PRaM and ATP in the areas of assembly, contacting, encasing and measuring of semiconductor elements and, further, in the sphere of handling semiconductor materials, chips or cassettes. The nature of technological operations also predetermines the technological properties of PRaM: high precision at great speed, increased resistance against the effects of dusty and toxic media, a high degree of adaptavity and reliability characteristics. The mentioned robotic system is also finding wide application in plants of the concern TESLA-Electronic Parts.

A brief outline and informative presentation can hardly exhaust the currently already very complicated problems attendant to the development, production and application of PRaM in our sector. Thus, let the kind reader view this editorial as a mere contribution toward more specific insight into the too generalized form of information so frequently offered.

Digital Integrated Circuits

Prague SDELOVACI TECHNIKA in Czech No 12, 1983 pp 443-448

[Article by Eng Pavel Polasek and Eng Josef Halamik: "Custom-Designed Digital Integrated Circuits From the TESLA Concern Enterprise in Roznov"]

[Text] Introduction

The rapid development of electronics that affects areas ranging from the most varied sectors of industry to the area of consumer products is forcing final producers to innovate their products to make them compatible with

the technical level prevalent on the current international market. The requirement pointed up in recent times by economy measures in the sphere of energy and materials can be met primarily by the wide application of modern monolithic integrated circuits. The TESLA Concern Enterprise in Roznov is turning out at the present time a wide assortment of bipolar digital integrated circuits which together with unipolar circuits (and/or integrated circuits produced in CEMA countries) provide summarily a good parts base for our electrotechnical industry. The mentioned parts provide at the present time a basis for devising electronic connections almost at random, but in some cases achieving the desired function is too complicated, calling for a considerable number of integrated circuits of SSI and MSI complexity. The specified reasons (as well as other technical aspects) led to the formulation of a task which had as its objective the devising of a methodology for the design and production of semi-custom and custom-designed digital integrated circuits. The following information presents an outline of the current status of how these circuits are dealt with by TESLA Roznov and, at the same time, provides interested parties with basic facts attendant to the procedures involved in the design of an eventual customer-oriented integrated circuit. In view of the fact that development of semi-custom design of IO [integrated circuits] is in its initial stage, information describing the circuits is presented merely in the form of an outline. As soon as semi-custom designed IO are ready for routine applications, more detailed information will be published.

Semi-Custom Designed Integrated Circuits

The term semi-custom designed integrated circuits denotes integrated circuits of an all-purpose character [5] in which the production of chips is completed by using one to three custom-design stencil-type exposure masks. This involves in most cases interconnecting masks that are used to devise the circuit function desired by the customer. Silicon plates with an all-purpose gate matrix are produced up to the already-mentioned interconnection level and can be kept at this phase in storage, after which a customer's specific demands can be met very expediently.

Dealt with in the first phase at TESLA Roznov are all-purpose logic fields containing 200 logic gates on a chip; in the next phase the all-purpose chip will be expanded to 1,000 logic gates. The employed technology facilitates the devising of fast gates with a delay of approximately 5 ns and power dissipation of 1 mW. In assembly it will be possible to make use of the entire assortment of the currently used casings with 16, 18, 20, 24, 28 and 40 outlets. In addition to the development of the mentioned technology, a general methodology for design of the mentioned gate fields is currently under way in collaboration with the VUMS [Research Institute for Mathematical Machines] Prague and VUVT [Research Institute of Computer Technology] Zilina. Specific efforts are oriented toward design of the gate matrix configuration, design of a logical diagram and its simulation, conversion of the logic design into a two-level interconnection of the gate matrix, the manner of data sharing between customer and producer, testing of chips and of encased circuits as well as the resolution of economic and time problems. The key advantages offered by the mentioned circuits include the potential for small series production, short time lapse between order and providing of samples and, of course, higher

technical level of design for the required function. The users of logic fields will come primarily from among computer technology researchers, but demands of additional customers from other branches of industry can also be met.

Custom-Designed Integrated Circuits (ZIO)

The area of fully custom-designed integrated circuits has been worked out in TESLA Roznov in closer detail than that of semi-custom design of IO and has become a routine operation by now. In selecting technology for ZIO, consideration was given, among other things, to the problem of the potential complexity of circuits and, consequently, a search was on for technology that would make it possible to achieve a degree of integration of LSI or VLSI level. In view of the fact that semi-custom designed IO in the form of Schottky TTL circuits with low power input are provided for high-speed applications particularly in the area of computer technology, design of ZIO was oriented toward the area of peripheral devices for computer technology and, eventually, some other industrial applications that do not call for top speed. For the stated reasons the integrated injection logic (I^2L) which adequately meets the specified requirements was selected for ZIO design. I^2L is used abroad in combination with analog circuits as well as in the design of exclusively digital IO of a high degree of complexity [4]. It is used due primarily to the key advantages it offers, i.e., very low power dissipation, high resistance to interference, range of operational temperatures of the 54 series and potential for design of highly integrated circuits. Since many modifications of the I^2L structure have been developed, the following text offers a brief description of the I^2L structure used in TESLA Roznov.

Basic Properties of I^2L

The basic structural element of I^2L is a single output, multiple output inverter constituted by a multicollector NPN transistor operating in inverse mode with its base being fed by a power source--an injector [3]. The injector is constituted by a lateral PNP transistor. As can be seen in Figure 1, the structure can be devised with great advantage also topologically. It is devised by means of five exposure masks.

The basic I^2L gate can be used in a wide range of supply currents, but its dynamic properties are determined by the level of the feed current. In addition to the feed current, the dynamic properties of gates are determined by structural design, i.e., distance between collector or contact from the injector, the mutual relative position of collectors and the base contact as well as by other design principles. There is a total of 176 structural variants of gates and for purposes of logic simulation taking into account the specific topology of gates it became necessary to determine the dynamic parameters t_{pLH} and t_{pHL} of all 176 variants. For the sake of illustration, Figure 2 shows several basic structural variants of I^2L gates and in individual collectors their dynamic parameters apply for the nominal value of the gate feed current which was set for ZIO at 100 μA per gate. From the configuration of the I^2L gate it follows

that--contrary to other logic systems that use a multi-input single-output gates--the I^2L is suitable for use in logic connections with one input and several outputs. I^2L gates can be connected directly in succession, whereby the basic condition for functioning is that the preceding circuit take up the entire feed current of the subsequent inverter. In view of the fact that gate outputs have the character of an "open collector," it is possible to connect outputs very simply and form a function called "assembly AND" (product on conductors). Using the latter and other gate connections makes it possible easily to devise the basic logic functions OR, NOR, AND, and NAND. An example of devising of basic logic functions in I^2L is shown in Figure 3.

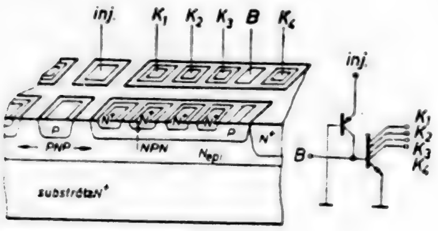


Figure 1. Horizontal and vertical I^2L structure

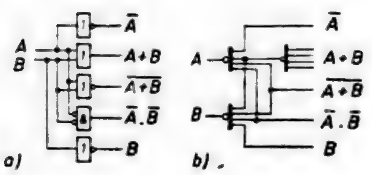


Figure 2. Dynamic parameters of basic structural variants of I^2L gates: K--collector, B--base, I--injector

Figure 3. Devising of basic logic functions, a) logic diagram in TTL, b) equivalent diagram in I^2L

Catalogue of I^2L Functional Blocks

The ZIO design concept in TESLA Roznov was based on the so-called catalogue of I^2L functional blocks. It contains a number of basic logic I^2L circuits which from the viewpoint of assortment and complexity can be compared to the basic series of logical TTL circuits. The catalogue is to enable the customer to select custom-design LSI or VLSI integrated circuits in the same way as the design of printed circuit plates on the basis of the existing catalogue of TTL logic circuits. The catalogue of I^2L functional blocks is not closed and in case of need it can be supplemented by new functional blocks required for any given custom-designed circuit. However, new blocks will be added to the catalogue only when their all-purpose use in other ZIO is possible. Functional blocks used to meet a single purpose in only one specific ZIO will not be incorporated into the catalogue.

A five-digit alphanumeric code was selected for designation of functional blocks compiled in accordance with the following system:

First symbol--letter:

I--denotes I^2L circuits;

Second symbol--letter:

B--combination circuits,

C--coders, decoders,

E--I^2L oscillators,

H--gates,

I--TTL - I^2L input converters,

K--flip-flop (sequential) circuits,

L--multilevel logic,

M--memories, PLA,

O--I^2L - TTL output converters,

R--resistances,

T--timing circuits,

V--input/output converter,

Z--special custom-designed blocks;

Third symbol--numeral:

0--blocks made up exclusively of basic gates,

1--"higher blocks" made up of gates and blocks with initial numeral 0,

2--"higher blocks of second category" made up of gates and blocks with initial numerals 0 and 1;

Fourth and fifth symbol--numeral:

designates serial number of block in the given category.

The catalogue of functional blocks comes in two versions--external, offered routinely to customers, and internal (operational), which also contains

the topology of functional blocks and other data not used by a substantial majority of customers. Figures 4 and 5 illustrate the contents of the external and internal operational catalogue page for the IK001 flip-flop circuit.

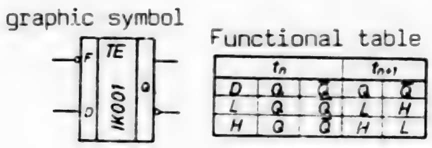


Figure 4. Contents of external catalogue page for the IK001 functional block; function of outlets: F--clock input (act. descending edge), D--data input, Q--data output

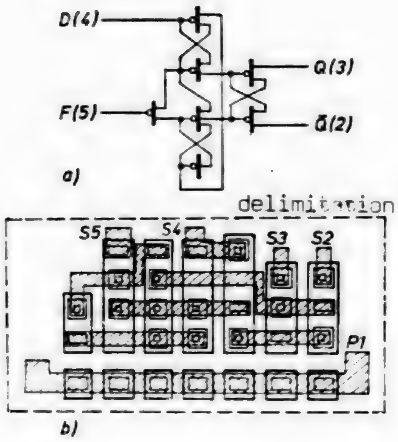


Figure 5. Additional data contained in the internal (operational) catalogue page for the IK001 functional block; a) electric wiring diagram, b) topology

Another part of the operational catalogue page is a table specifying the position of connecting points (drops) in reference to point 1 in steps of the uniform screen roster. All functional blocks are designed in this symbolic form represented by delineation of the block and connecting points. This symbolic representation of the blocks is then used with advantage in the specific design of the chip's topology, i.e., distribution and interconnection of functional blocks over the area of the chip of a specific ZIO, and promotes improved automation of operations in the design of integrated circuits.

At the present time the catalogue of I^2L functional blocks contains the functional blocks specified below (the assortment of flip-flop circuits is shown in Table 1). Annotations to Table 1:

T (D) "with data"--T (D) type flip-flop circuit with potential for asynchronous presetting of data on outputs Q, $\bar{Q}$;

$\bar{J}$-$\bar{K}$ sym. --symmetrically controlled J-K type flip-flop circuits (containing circuits $\bar{J}$-$\bar{K}$ and J-K);

$\bar{J}$-$\bar{K}$ asym. --asymmetrically controlled J-K type flip-flop circuits (containing $\bar{J}$-K and J-$\bar{K}$ circuits);

TEF --flip-flop circuit controlled by descending edge;

TER --flip-flop circuit controlled by ascending edge;

MS --flip-flop circuit of the type "master-slave";

TL --flip-flop circuit of the type "latch."

Table 1. Flip-flop Circuits

Type of flip-flop c.	Type of Control	Function of flip-flop circuit				
		basic	with zeroing	with setting	w/zer. & set.	with blocking
D	TEF	IK001	IK002	IK003	IK004	
D	TL	IK009				
D	MS					IK005
D "with data"	TEF	IK011				
T	TEF	IK021	IK022	IK023	IK024	
T	TER	IK025				
T "with data"	TEF	IK031	IK032			IK035
$\overline{J}$—$\overline{K}$ sym.	TEF	IK041	IK042	IK043	IK044	
$\overline{J}$—$\overline{K}$ asym.	TEF	IK051	IK052	IK053	IK054	
$\overline{J}$—$\overline{K}$ sym.	MS		IK046		IK048	

The entire assortment of Table 1 can be used in the design of ZIO; variants of flip-flop circuits that have not been assigned a 5-digit designation as yet will be added to the table as needed.

Other functional blocks:

IK101--binary 4-bit bidirectional counter with data setting

IK102--binary divider (time)

IK104--asynchronous binary decadic counter with zero setting

IK106--quadridecadic frequency divider with zero setting

IK108--asynchronous 6x counter in BCD code with zero setting

IK109--binary 8-bit bidirectional counter with data setting

IK110--programmable frequency divider

IK111--9-bit programmable frequency divider (:1 to :511)

IB001--4-input multiplex

IB003--derivation element

IB004--EXCLUSIVE-OR gate

IB005--equivalency comparator

IB006--threshold circuit 2 out of 3

IB007--EXCLUSIVE-OR equivalent gate

IB009--1-bit full adder

IB010--double EXCLUSIVE-OR

IB011--generator of accelerated transmission--4 orders

IB013--2-bit full adder

IB015--generator of accelerated transmission--2 orders

IB017--2-bit comparator

IB019--controlled BCD decoder on 1 of 4

IB021--logic products matrix 2 x 2

IB022--logic products matrix 2 x 3

IB023--logic products matrix 3 x 3

IB024--4x two-input multiplex

IB027--4-bit direct, negated, zeroing, setting element

IB103--4-bit comparator

IB105--8-bit coincidence comparator

IB106--full 8-bit binary adder with CLA

IB107--busbar priority generator

IC001--decadic/binary coder

IC003--decoder of BCD code to decadic

IC005--decoder of code excess 3 to decadic

IC007--decoder of code excess 3 Gray to decadic

IC009--decoder of binary code to code 7--of segment display, com. cathode, (IC010--com. anode, IC013--hexad. display)

IE001--current-controlled oscillator with blocking

IH005--multioutput inverter

IL001--threshold circuit 1 of N

IL060--6-stage voltage-level indicator

IM001--decodable memory of constants

IM100--programmable logic field

II002--input TTL-I^2L converter

IO002--output I^2L-TTL converter

IV004--input/output converter

Properties of Basic Functional Blocks

As already stated, we envision the major part of I^2L ZIO applications in areas not too demanding on dynamic properties. In general, it can be said that from the viewpoint of dynamic properties the I^2L used in TESLA Roznov for ZIO can be compared to CMOS circuits--Figures 6 and 7 show the results of measuring of the dynamic properties of block IK025. In view of the fact that I^2L ZIO are designed as compatible with TTL integrated circuits, converters TTL-I^2L and I^2L-TTL belong among the basic functional blocks. The input TTL-I^2L converter (Figure 8) converts TTL voltage levels to internal current I^2L decisionmaking levels. The input transistor T_1 operates in inverse mode and, contrary to the I^2L gate, it has no power source in its base (this accounts for the reverse state of unconnected input of I^2L ZIO than is the case with TTL). Figures 8 and 9 show the wiring and transfer characteristics of the input TTL-I^2L converter.

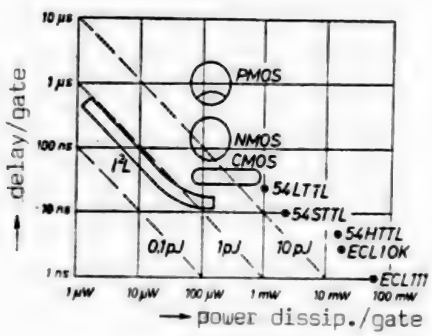


Figure 6. Position of I^2L technologies in a number of monolithic IO technologies

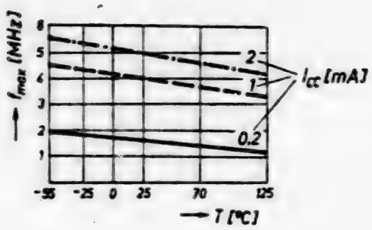


Figure 7. Dependence $f_{max} = f(T)$ for two IK025 blocks in series

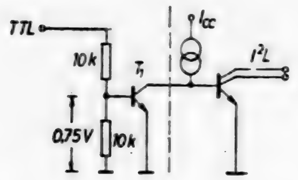


Figure 8. Wiring of TTL-I^2L input converter

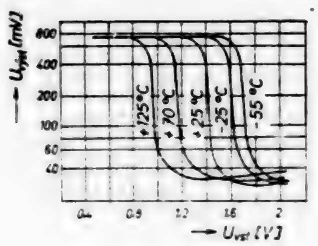


Figure 9. Transfer characteristics of the TTL-I^2L converter

With regard to the dynamic properties of the input converter, they were verified for various levels of input voltage, various levels of loading current and the entire temperature range of the MH54 series. In brief summary, for the typical value of parameter $U_{vst(1)}$ = 3.2 V, loading current of 100 µA and ambient temperature of 25°C the delay t_{pHL} is ~21 and delay t_{pLH} is ~95 ns.

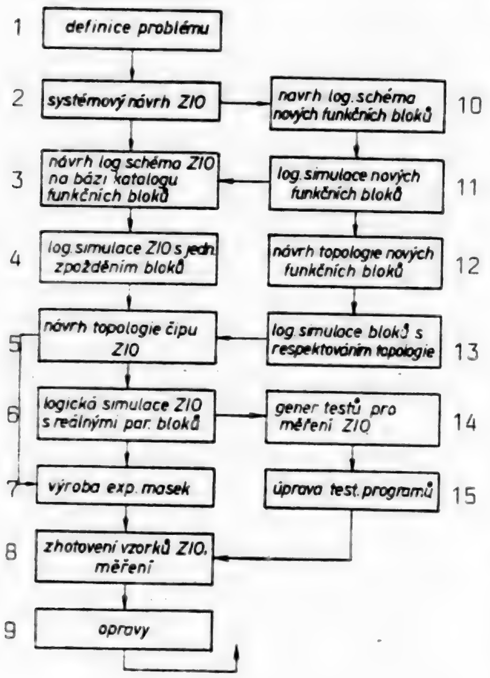
The output I^2L-TTL converter is a system of two or three I^2L gates that are standard from the circuit viewpoint, but are designed so that the last gate in state L can be loaded similarly to the TTL outputs, i.e., by 16 mA. Typical for the loading current of 16 mA and temperature of 25°C--specified for nominal operational conditions--are delay values t_{pLH} ~130 ns and t_{pHL} ~100 ns. However, custom-design IO can be designed from the viewpoint of loading current on the output at random in a range of up to 50 mA, but for higher values of current it is necessary to take into account higher delay values. ZIO outputs have the nature of TTL outputs with an open collector.

Methodology for Custom Design of IO

The resolution of a number of tasks in the area of technology and design created in TESLA Roznov the prerequisites for custom-design of IO. Mastering the technology at the level of pilot production affords adequate flexibility in meeting the required volumes of ZIO. In the area of design it became possible to come up with a closed ZIO system which--even though software is being constantly supplemented--is functional and was checked

during design of specific ZIO. On the basis of available experience, the optimum procedure for the design of a general ZIO can be briefly defined in accordance with Figure 10.

Figure 10. Sequence followed in the design of general ZIO



Key:

1. Definition of the problem
2. Systemic ZIO design
3. ZIO logic diagram based on catalogue of functional blocks
4. ZIO logic simulation with un. block delay
5. Proposed ZIO chip topology
6. Logic ZIO simulation with real par. blocks
7. Production of exposure masks
8. Completion of ZIO samples, measurements
9. Corrections and repairs
10. Proposed logic diagram of new functional blocks
11. Logic simulation of new functional blocks
12. Proposed topology of new functional blocks
13. Logic simulation of blocks with respect to topology
14. Generation of tests for ZIO measurements
15. Adaptation of test programs

The sequence followed in design presented above offers only a rough summary of operations that have to be performed in the course of ZIO development. It also does not contain any dividing line between the operations that have to be performed on the part of the customer and producer, respectively. The extent of operations performed on the part of the customer depends on the level of his resources and possibilities; depending on the extent of participation in ZIO development, customers may be divided into three groups:

a) A customer who has at his disposal no specialists in the area of electronic circuit design. He defines the required properties of IO merely by verbal description of the external function and does not participate in proposing the functional diagram or subsequent operations relevant to the design. The responsibility for the design of a circuit meeting the desired function is borne by the producer.

b) A customer who contracts for development on the basis of the catalogue of functional I^2L blocks in the form of an overall logic diagram, description of function, and/or the truth table and the demands on dynamic properties. The responsibility for the correctness of the logic diagram is borne by the contracting customer and, depending on the possibilities open to him, simulation of the circuit's function is carried out on a computer. The producer starts his part of operations by proposing the ZIO topology.

c) A customer who contracts for development of ZIO on the basis of the catalogue of functional I^2L blocks in the form of a logic diagram, description of function and/or truth table, demands on dynamic properties and proposed chip topology at functional block level (proposed distribution and interconnection of functional blocks). Such a customer must be capable of converting the data describing the chip topology into the design system of TESLA Roznov. The producer starts operations by optimizing the topology of functional blocks and transferring the proposed design down to the level of detailed topology of I^2L gates. Logic function at functional block level must be simulated on a computer.

This classification--which has been proven realistic by our experience so far--provides at least a partial insight into the customer's potential participation in ZIO design. It stands to reason that most customers will be found in group b, others will fall in groups a or c. As an example of a customer from group c can be cited the VUVT Zilinia, which is capable of designing I^2L ZIO down to the level of chip topology. That means that the VUVT Zilina can enter with chip topology data into the design system of TESLA Roznov where completion of the proposed design will be substantially less labor-intensive and time-consuming. Such a system of operation is based on the so-called circuit phase programs which make it possible to use functional blocks in symbolic form represented by delimitation of the block and connecting points. An example of a chip design by means of circuit phase programs is shown in Figure 11.

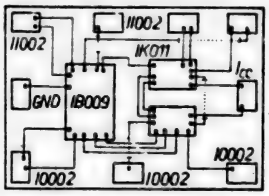


Figure 11. Example showing use of functional blocks in symbolic form

In view of the fact that the custom and semi-custom design approach to the design of microelectronic circuits is growing increasingly in importance worldwide, the viable approach would be to establish in the CSSR more work centers of type c in the coming years. For this reason it would be advisable to develop hardware and software for potential customers of type c with a view toward compatibility with producers of microelectronic elements. A similar system in the area of semi-custom design of circuits has been established in the GDR.

In addition to the extent of the customer's participation, also of importance to the estimation of the chronological progress of ZIO design is the complexity of the ZIO being developed. Limitations from the viewpoint of maximum chip size and usability of chip area (i.e., ratio between chip area covered by I^2L gates to the area taken up by the interconnecting network, contact surfaces, etc.) indicates for the extant technology the maximum number of gates per chip to be approximately 1,500. Taking into consideration the classification of customers and complexity of circuits, chronological problems attendant to ZIO design are summarized in Table 2, which

shows the number of months that elapsed between the start of operations on a given ZIO in TESLA Roznov till completion of the first sample. In view of the high degree of integration and complexity of the technological procedure in the production of IO, in most cases the initial samples cannot be expected to function faultlessly. Thus, the overall duration of development will depend primarily on the quality of the basic logic design (logic simulation) and its errorless transfer into topology.

Current State of ZIO Design in TESLA Roznov

The development of the first I^2L ZIO in TESLA Roznov was completed in 1980. On the basis of a demand made by the concern enterprise Zbrojovka Brno, a coder for contactless keyboards MH1KK1 was developed. The circuit performs the function of a converter of code 1 of 16 to a 4-bit binary code and is provided with outputs that confirm the validity of the code information or indicate faulty information (depressing of two pushbuttons simultaneously, etc.) and blocking it. The MH1KK1 integrated circuit constitutes a part of the TESLA Roznov production program and detailed information is available in the catalogue of TESLA semiconductor parts. The circuit was designed at gate level before the catalogue of functional blocks became available--its complexity is 145 I^2L gates.

Complexity / Customer	200 gates	400 gates	800 gates	1500 gates
A	10	12	16	
B	8	10	13	18
C	6	8	10	14

Table 2. Duration of ZIO development (months)

Other ZIO the development of which has been completed at the present time include the MH100 interpolator developed for control systems of machine tools, the contractor being the Research Institutes for Machine Tools and Machining in Prague. It is a DDA interpolator of the register type with length of data register variable up to 24 bits. Selectable register length makes it possible to accelerate interpolation for circles of smaller radii while the precision of interpolation remains unchanged. The circuit facilitates the interpolation of a circular path with a maximum radius of 2^{24} of uniform steps (μm), i.e., about 16 m at the required machining speed of 10 m/s and, further, linear interpolation, eventually parabolic interpolation. The MH100 IO is encased in a DIL casing with 28 outlets, its typical feed current is 120 mA, power dissipation 150 mW. Functioning of the circuit was verified also at feed current lower by one order (without any demands on dynamic properties) and in a temperature range of -55 to +125°C. The MH100 circuit contains 1,145 I^2L gates. Figures 12 and 13 show the functional diagram and wiring of outlets of the MH100 IO.

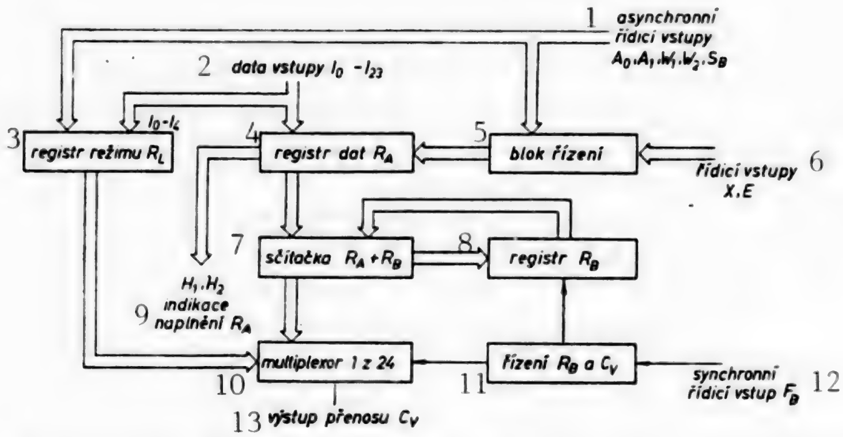


Figure 12. Functional diagram of the MH100 circular interpolator

Key:

1. Asynchronous control inputs
2. Data inputs
3. Mode register
4. Data register
5. Control block
6. Control inputs
7. Adder
8. Register
9. Saturation indicator
10. Multiplex
11. Control
12. Synchronous control input
13. Transmission output

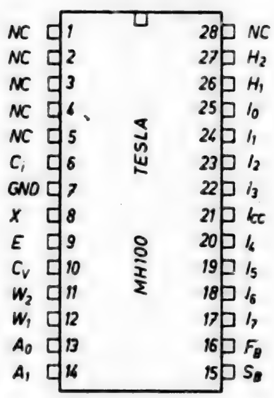


Figure 13. Wiring of casing and functions of MH100 outlets

I_o through I_7--data inputs into R_A; W_1 and W_2--recording inputs; A_o and A_1--addressing inputs R_{Ao} through R_{A7}, R_{A8} through R_{A15} and R_{A16} through R_{A18}; E--timing input for change control of R_{Ao} +1 and -1; X--counting direction input (+1, -1); F_B--timing input (entry into R_B); H_1 and H_2--indication of R_A regulation state; C_V--transmission output; S_B--zeroing input; C_i--testing input

Another I^2L ZIO the development of which had been completed is the MH102 multiplier contracted for design from the VUVT Zilina for use in the SM 50/40 microcomputer system, which is based on the 8080 microprocessor. The basic mode of operation is multiplication of two 8-bit numbers with a 16-bit product. In other modes the product can be rounded off to 8 bits, and also multiply two 7-bit numbers bearing a sign. Use of the MH102 makes it possible to substitute program multiplication which lasts about 1 ms by technical multiplication which occurs within 2 s, making the microprocessor system suitable for control of continuous processes. The MH102 can be used in all microcomputer systems based on the 8080 and 8085 microprocessors. The MH102 IO was designed on the basis of the modular system of standard I^2L functional blocks by means of the already-mentioned

circuit phase. The circuit is encased in a standard 16-outlet plasting casing, its typical feed current is 120 mA, power dissipation 150 mW. The MH102 includes 970 I^2L gates. Figures 14 and 15 show the wiring of the casing, the function of outlets and the circuit's diagram.

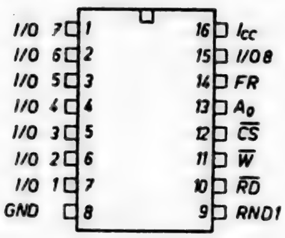


Figure 14. Wiring of Casing and Functions of MH102 outlets
I/O_1 -/ I $/O_2$--input/output circuits; $\overline{CS}$--circuit implements; W--entry into circuit; $\overline{RD}$--readout from circuit; A_0--byte selection; FR--multiplication format; RND1--rounding off

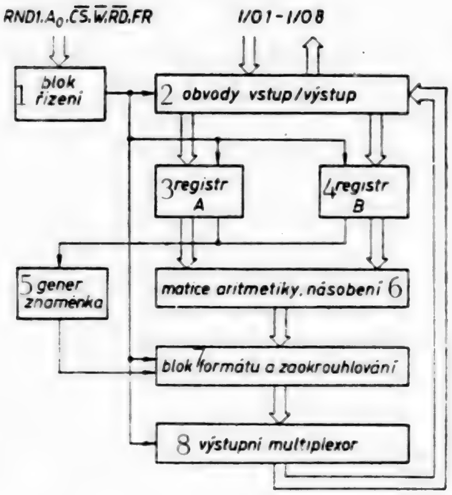


Figure 15. Functional diagram of the MH102 multiplier hardware
Key:
1. Control block
2. Input/output circuits
3. Register
4. Register
5. Sign generator
6. Arithmetic matrix, multiplication
7. Format and rounding off block
8. Output multiplex

The fourth in sequence and the I^2L ZIO currently under development is the MH101 cyclic code generator. The MH101 IO provides for the transmission of information through encoding by means of one of the four selected polynomials: $x^8 + 1$, $x^{16} + x^{15} + x^2 + 1$, $x^{16} + x^{12} + x^5 + 1$, $x^{14} + x^{10} + x^3 + 1$. The circuit processes either serial data from input SCRCIN or parallel data from input-output circuits. In using parallel data the last, eighth bit can be replaced by an odd or even parity bit which is computed out of the first seven bits by the paritator. In parallel operation the data are fed in batches of eight; during serial operation the data pass through continuously. The MH101 IO was contracted for by the VUMS Prague and its design was participated in (in the area of chip topology) by the VUVT Zilina. The MH101 IO contains 500 I^2L gates, is encased in a 16-outlet plastic casing and its typical feed current is 50 mA. Figures 16 and 17 show wiring of the outlets and functional diagram of the MH101 circuit.

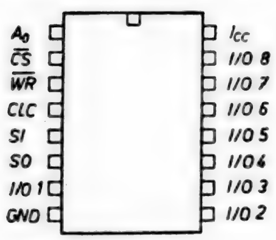


Figure 16. Wiring of casing and function of MH101 outlets
I/O_1 through I/O_8--input-output terminals for parallel data; $\overline{CS}$--circuit fittings; $\overline{WR}$--input recording-readout; A_0--mode selection input; SI-SCRCOUT--serial data output

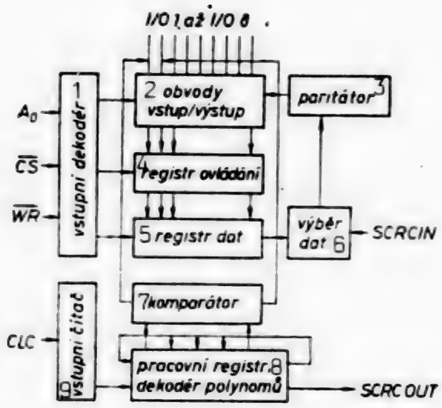


Figure 17. Functional diagram of MH101 CRC controller

Key:
1. Input decoder
2. Input/output circuits
3. Paritator
4. Control register
5. Data register
6. Data selection
7. Comparator
8. Operational register, decoder of polynomials

Basic development of MH100 and MH102 IO has been concluded and the circuits may be ordered from TESLA Roznov. The desired number of samples will be sent to interested parties by return mail. In view of the fact that circuits MH100 and MH102 have not been entered into the catalogue of TESLA semiconductor components as yet, a detailed description of the function and technical specifications of the circuits can be obtained in the form of a technical report.

Potential for Expanding the Assortment of Custom-Designed I^2L IO

In addition to custom-designed IO contracted by a specific contractor as described in closer detail in the preceding part, in the course of development of methodology for ZIO design there were verified other circuit units which in view of their all-purpose nature have the prerequisite for finding application with many users in various fields. The mentioned structures have been, for all practical purposes, devised and measured; however, additional efforts (i.e., final circuit design, definitive wiring of the casing, etc.) will be continued only if required to meet the requirements of final producers in TESLA Roznov. Closer details regarding individual circuit structures are provided in the subsequent text.

Memory-Decoder-Excitors

The mentioned circuit structure is formed by a 4-bit input memory register of the "latch" type, the output 4-bit binary information of which is decoded in the full decoder into the code of 7-segment displays in hexadecimal representation. The output circuits can perform some of the following functions:

a) Excitors of 7-segment luminous displays with a common anode, where the output currents have the character of current sources switching constant current. Thus, the circuit can switch segment cathodes without any auxiliary resistances. DIO casing--16 outlets.

b) Excitors of 7-segment luminous displays with a common cathode. DIL casing--16 outlets.

c) Excitors of 7-segment liquid crystal displays (LCD) using an additional phasing output outlet. DIL casing--18 outlets.

The circuit contains additional auxiliary outlets, such as RBI and RBO, serving to suppress nonfunctional zeroes during cascade sequencing of digit generators. In cases where memories are made to operate in continuous mode (by means of input F) the mentioned circuit serves only as decoder of BCD into 7-segment hexadecimal code. The resultant display is shown in Figure 18. The circuit contains 120 I^2L gates, the feed current for versions a) and b) is 5 to 15 mA, depending on the switched current, for version c) it is 50 to 100 μA.

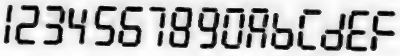


Figure 18. Final display of hexadecimal code

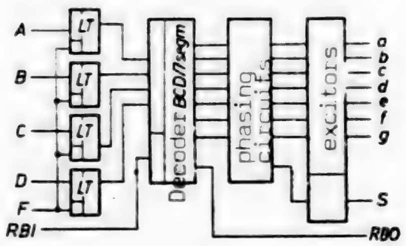


Figure 19. Functional diagram of the structure "memory-decoder-excitors"

2 1/2 Decadic BCD Counter--Memory--Decoder of BCD into 7-Segment Symbol--Excitors of 2 1/2-Digit Luminous Display

The circuit counts input pulses from input f_i in the 2 1/2 decadic BCD counter. The immediate state of the chain of counters can be transcribed by means of control input L into "latch"-type memories. Binary decadic information stored in memories is decoded into the code of 7-segment displays and the output circuits excite the luminous displays of the common anode type--Figure 20.

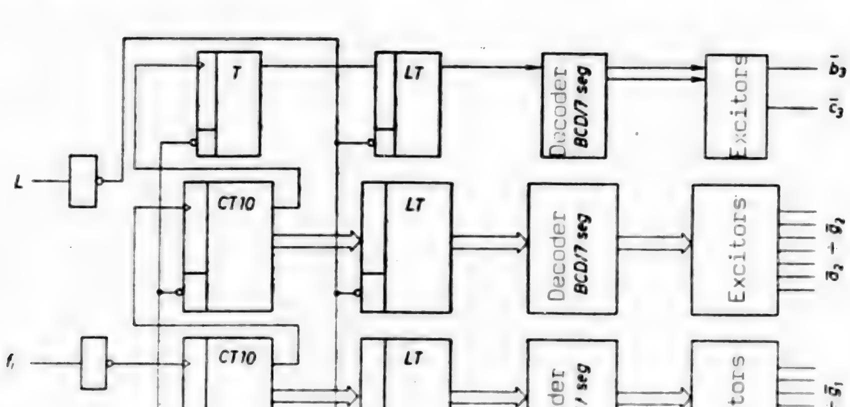


Figure 20. Functional diagram of the structure "counter-memory-decoder-excitors"

The cathodes of individual segments are switched directly by constant current circuits without serial resistances; the switching current of segments can be adjusted. The cascade of input counters can be asynchronously zeroed by level H on control input CL. If memories are in continuous mode, displays indicate the immediate state of the cascade of BCD counters. Another verified version was only a two-decadic chain counter-decoder-excitors with led-out transmission of the upper decade in a DIL casing with 20 outlets. The mentioned circuits can be arranged consecutively in order to form a randomly long cascade. The circuit contains 230 I^2L gates, its feed current ranges between 10 to 35 mA depending on the switched current.

9-Bit Programmable Frequency Divider--Figure 21

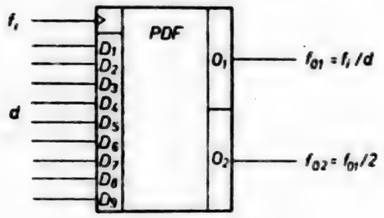


Figure 21. Equivalent diagram of programmable frequency divider

The circuit facilitates the division of input frequency f_i by the number 1 through 511. The number by which the circuit divides the input frequency is set in binary form on 9 data inputs. The output pattern of f_{01} is in the form of negative pulses. The circuit has a second output on which the frequency f_{01} via a T-type flip-flop circuit is divided by alternating 1:1. The circuit contains 120 I^2L gates, its feed current is 0.5 to 15 mA.

Binary Divider (Watch-Type)--Figure 22

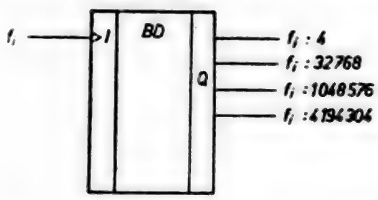


Figure 22. Equivalent diagram of binary divider

The binary divider is formed by a cascade of 22 flip-flop circuits of the type T; from the requisite stages of the cascade are led out outputs on which the input frequency is divided by the numbers: 4, 32, 768, 1,048, 576, 4,194, 304. This makes it possible to obtain from the majority of the used watch crystal cut sections an output frequency of 1 Hz. With an eventual variant of the circuit it is possible to lead out additional accessible frequencies. The circuit contains 140 I^2L gates, the feed current for input frequency of 4.1 MHz is 8 mA, for 1.1 it is 1 mA, for 32 kHz it is 80 μA. The voltage on fed outputs ranges between 0.8 and 1.2 V.

4-Decadic Frequency Divider, Decadic Counter--Figure 23

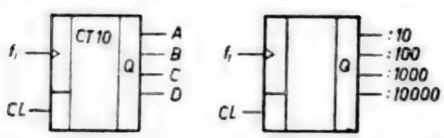


Figure 23. Equivalent diagram of 4-decadic divider and decadic counter

The mentioned circuit structure contains two functional units--a 4-decadic frequency divider with zeroing and an independent decadic counter with zero setting. On four outputs of the decadic divider we obtain the input frequency divided by 10, 100, 1,000 and 10,000. The independent decadic counter counts input pulses in binary decadic code; the counter can be asynchronously set to zero by level H on input CL.

The circuit can operate in various modes of current supply depending on the requirements on the processed input frequency. For the maximum input frequency of 4 MHz the feed current of the 4-decadic divider is 15 mA, and that of the decadic counter 3 mA. With lowering of the feed current the function of the circuit remains unchanged, and the maximum value of the processed input frequency decreases. For example, the circuit processes a frequency of 1 MHz at feed current of 2 mA for the 4-decadic divider and 0.4 mA for the BCD counter.

In case of need it is possible to devise other variants of decadic counters or dividers. For example, a cascade of 12 decadic dividers providing the frequency base for measuring devices, a chain of six decadic BCD counters usable in systems for frequency measurements, etc.

8-Bit Coincidence Comparator--Figure 24

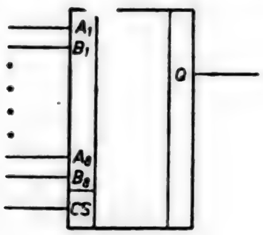


Figure 24. Equivalent diagram of coincidence comparator

The 8-bit coincidence comparator makes it possible to compare two 8-bit words, the sign of coincidence being level H at output Q. In view of the fact that outputs are of the open collector type, more circuits can be arranged in parallel to form 16- or 24-bit coincidence comparators. Another verified variant was that of a circuit where the compared word is stored in the "latch" type 8-bit memory on the same chip. This version makes it possible to form 8-, 16- and 24-bit comparators comparing the state on an 8-, 16- and 24-bit busbar with the word stored in the 8-, 16- and 24-bit memory. If the control input for entry into memory is set at level H, the memory switches to continuous mode and the circuit performs the previously mentioned function. Depending on the demand on speed of comparison the feed current can be selected in a range of 50 μA to 4 mA.

Conclusion

The mentioned examples of expansion of many custom-designed digital I^2L IO are relatively simple and were mentioned primarily to point out areas in which I^2L application can offer some advantages. The key objective of tasks dealt with in TESLA Roznov over the past 2 years in the area of

custom-designed IO was to work out a methodology for ZIO design, to compile a catalogue of functional blocks, to expand software for design and logic simulation of ZIO and to verify the potential for cooperation with customers. The mentioned tasks have been resolved to an adequate extent and it is up to the producers of finished electronic systems how they will avail themselves of the mentioned new possibilities in design of IO.

BIBLIOGRAPHY

1. Crippen et al, "High-Performance Integrated Injection Logic: A Microprogram Sequencer Built With I^3L," IEEE JOURNAL OF SOLID STATE CIRCUITS, Vol SC-11, No 5, 1976.

2. Mulder Cor, "High Speed Integrated Injection Logic (I^2L)," IEEE JOURNAL OF SOLID STATE CIRCUITS, Vol SC-11, No 3, 1976.

3. Blackstone, S.C. et al, "A Comparison of High Speed I^2L Structures," IEEE JOURNAL OF SOLID STATE CIRCUITS, Vol SC-13, No 6, 1978.

4. Blauschild, R.A. et al, "A Single Chip I^2L PCM Codec," IEEE JOURNAL OF SOLID STATE CIRCUITS, Vol SC-14, No 1, 1979.

5. Application Note Exar: Semi-Custom LSI Design With I^2L Gate Arrays.

GDR Semiconductor Parts

Prague SDELOVACI TECHNIKA in Czech No 2, 4, 6, 7, 12, 1983

[Article by Eng. Jaroslav Tolasz: "New Semiconductor Parts From the GDR"]

[No 2, Feb 1983 p 59]

[Excerpt] [Part 1] Microelectronics is proving that on an international scale it is becoming an increasingly important factor in the scientific and technological progress of all spheres of economic and public life in the sense that it keeps improving the standard of living of the inhabitants of all CEMA countries. This fact is promoted by the production program of the Microelectronics Combine [VEB Kombinat Mikroelektronik] in the GDR, which has a wealth of experience in the development and production of active electronic components. The latest findings of scientific and technological research form a solid base for the high-capacity consortium of an association of producers engaged in the production of semiconductor components of all types.

In 1982 the Microelectronics Combine introduced on the market new parts in an unprecedented volume, mainly from the area of bipolar and unipolar integrated circuits, transistors, diodes, optoelectronic components, basic materials for the production of semiconductor components, X-ray tubes and technological systems. In the subsequently offered information we describe new components, many interesting types of which will certainly be imported

by us within the framework of specialization of production and, outside of it, as a supplement to the assortment of TESLA production enterprises to enrich our electronic parts market.

To supplement the information about RFT semiconductor components that has been published over the past several years in SDELOVACI TECHNIKA, we list in Tables 1 through 3 an outline of all the published types of components, including an analogous type turned out by the world's producers. The tables should simplify searching through past issues of SDELOVACI TECHNIKA and expedite the search for alternate types.

Table 1. Outline of integrated RFT circuits published in SDELOVACI TECHNIKA 1/1976

Type	Worldwide Alternate
D100C,D	SN7400
D103C,D	SN7403
D110C,D	SN7410
D120C,D	SN7420
D122C,D	SN7522
D126C,D	SN7426
D130C,D	SN7430
D140C,D	SN7440
D146C,D	SN7446
D147C,D	SN7447
D150C,D	SN7450
D151C,D	SN7451
D153C,D	SN7453
D154C,D	SN7454
D160C,D	SN7460
D172C,D	SN7472
D174C	SN7474
D181C	SN7481
D191C	SN7491
D192C	SN74192
D193C	SN74193
D195C	SN7495
E100C	SN8400
E103C	SN8403
E110C	SN8410
E120C	SN8420
E122C	SN7522
E126C	SN8426
E130C	SN8430
E140C	SN8440
E146C	SN8446
E147C	SN8447
E150C	SN8450
E151C	SN8451
E153C	SN8453
E154C	SN8454
E160C	SN8460
E172C	SN8472
D200C	SN74H00
D201C	SN74H01
D204C	SN74H04
D210C	SN74H10
D220C	SN74H20
D230C	SN74H30
D240C	SN74H40
D251C	SN74H51
D254C	SN74H54
D274C	SN74H74
D491D	SN75491
D492D	SN75492
U101D	MEM1000
U102D	MEM1002
U103D	MEM1005
U104D	MEM1008
U106D	MEM1013
U107D	MEM1014
U108D	MEM1015
U109D	MEM1022
U311D	MEM3005PP
U352D	MEM3064B
unipol. trans.	MOS
U105D	MEM2001
SMY50	MEM511
SMY51	MEM550
SMY52	MEM517

Table 2. Outline of integrated circuits and discrete semiconductor parts published in SDELOVACI TECHNIKA 11 and 12/1981

Type	Worldwide Alternate
A232D	TDA2532
A255D	TDA2593
A277D	UAA180
A283D	TDA1083
B260D	TDA1060
A302D	MCC302
B308D	~TAA970
B318D	—
B461G	SAS261S4
B462G	SAS261
C520D	AD2020
D104D	SN7404N
D108D	SN7408N
D394D	—
D410D	—
U256C	—
U505D	—
U555D	—
U4001D	CD4001
U4011D	CD4011
U4012D	CD4012
U4023D	CD4023
U4030D	CD4030
VQ120	—
VQA25	—
VQA35	—
VQE21, VQE22	—
VQE23, VQE24	—
SP211	—
MB111	—
L110C	—
SY180	DSI10
SY180A	DS17
SY185	DSD17
SY330	BY211
SY335	BY201
SY360	1N4000—1N4007
SC307	BC307
SC308	BC308
SC309	BC309
SD600—SD602	—
SF369	BF469
SU160	BU208
SU167	BUY69B
SCE237	BCW71
SCE238	BCW31
SCE239	BCF32
SFE235	BFS18
SFE245	BFS20
SSE216	—
SSE219	BSV65

Table 3. Outline of articles about integrated RFT circuits published in SDELOVACI TECHNIKA (ST) in 1979-1982

Type	Ww Alternate	Description	ST No
U808D	8008	Mikroprocesor MOS s kanálem P	9/1979
A244D	TCA440C	Přijímač AM do 30 MHz	12/1979
A281D	TAA981	Zesilovač MF signálů AM/FM	1/1980
A240D	TBA440C	Zesilovač MF, dekodér, zesilovač obrazového kmitočtu	4/1980
A290D	MC1310P	Stereofonní dekodér	2/1981
U880D	Z80	Mikroprocesor 8 bitů	8/1982
U855D	Z80-PIO	Obvod paralelního styku vstup/výstup	8/1982
U856D	Z80-SIO	Obvod sériového styku vstup/výstup	8/1982
U857D	Z80-CTC	Generátor hodinových impulsů	8/1982
U858D	Z80-DMA	Obvod přímého přístupu do paměti	8/1982

Line-by-line key to the "Description" column:

Microprocessor MOS with channel P
Receiver AM to 30 MHz
Amplifier MF of AM/FM signals
Amplifier MF, decoder, video frequency amplifier
Stereophonic decoder
Microprocessor 8 bits
Circuit of parallel contact input/output
Circuit of series contact input/output
Hour pulse generator
Circuit for direct access to memory

[No 4, Apr 1983 pp 133-136]

[Text] [Part 3] Logical Integrated Circuits

The Semiconductor Plant (Halbleiterwerk) in Frankfurt on the Oder River is expanding the routinely produced assortment of TTL bipolar logical integrated circuits by new components. These include primarily the E104D set of six invertors (a variant of the worldwide type SN-8404N) and E108D set of four 2-input positive logic members NAND (variant SN8408N) designed for operation in a wider range of operational temperatures from approximately -25°C to +85°C.

The D351D, E351D Frequency Dividers

The Research and Technological Center for Microelectronics in Dresden is readying production of two integrated circuits by the I^{2}L technology. The types D351D and E351D are integrated dividers designed for expanding integrated circuits D355D and E355D or for general application as frequency dividers. The circuit has four dividing chains which can be combined by external connection for the requisite length, has outputs with an open collector, the divider's output signals have a keying ratio of 0.5, inputs and outputs of the circuit can be combined with TTL circuits. The divider's operation is asynchronous. In connection with circuits D355D and E355D the circuit makes it possible to achieve a delay time of up to 40 days. The functional group wiring of integrated circuits D351D and E351D is shown in Figure 24.

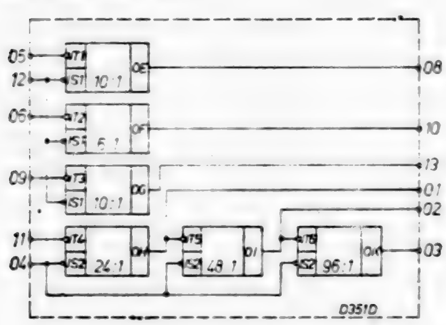


Figure 24. Functional group wiring of integrated circuits D351D, E351D

The integrated circuit consists of frequency dividers 10:1 (divider E), 6:1 (F), 10:1 (G) which have independent outputs and dividers 24:1 (H), 48:1 (I), 96:1 (K) which are interconnected in series, but with an additional output from each divider. The integrated circuit is in a plastic casing DIL with 2x seven outlets in two rows.

Functions of the individual outlets: 01--output of divider H, 02--output of divider I, 03--output of divider K, 04--inverting S input of dividers H, I and K, 05--input of divider E, 06--input of divider F, 07--grounding point, 08--output of divider E, 09--input of divider G, 10--output of divider F, 11--input of divider H, 12--inverting input of dividers E, F and G, 13--output of divider G, 14--positive feed voltage $+U_{cc}$. Schematic diagram and connection of outlets are shown in Figure 25.

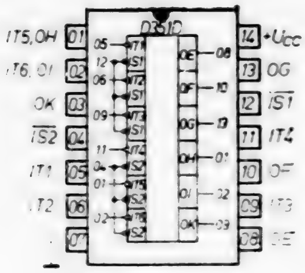


Figure 25. Schematic diagram and wiring of outlets if integrated circuits D351D, E251D

Limiting values of circuits D351D, E351D: feed voltage 0 to +8 V, input voltage minimum -0.8 V, maximum +7.25 V, input current max. 1 mA, power dissipation max. 400 mW, output voltage min. -0.5 V, max. +8 V. Range of ambient operational temperatures varies for both parts. The D351D can be operated from 0°C to +70°C, the E351D in an expanded range of −25°C to +85°C. Recommended operational conditions: feed voltage 4.75 to 7.25 V, input voltage at level L max. 0.8 V, at level H min. 2.4 V, output current at level L max. 4 mA. Output voltage at level H is max. 0.4 V at output current of 4 mA. Input frequency must not exceed max. of 105 kHz.

Timing Circuit D355D, E355D

Integrated circuits D355D, E355D combine in a common system an oscillator, a divider, control logic, a circuit for operational mode selection, a circuit for suppression of rebounding, an output for relay connection. Both parts find key application in electronic timing relays with switching time ranging from 100 ms to 10 min. The time can be prolonged in connection with integrated circuits D351D, E351D up to 40 days. These timing circuits are programmable into seven operational modes--delayed switching, count-controlled switching delay, time-lag circuit breaking, sawtooth oscillations, isolated pulse generation at steady input pulse, a stable multivibrator, divider by-pass. Delay time can be controlled by selection of internal or external oscillator frequency. The onset of the circuit's function is controlled by the descending pulse edge (H/L) on input IST. With connected feed voltage the circuit is automatically actuated at signal level L on input IST. Logical inputs and outputs of the circuit can be combined with TTL circuits. Integrated circuits are contained in the DIL plastic casing with 2x nine outlets in two rows.

Functions of individual outlets: 01--IT divider input, 02--OS oscillator output, 03--ORS relay output, 04--inverting output of ORS relay, 05--grounding point, 06--A divider output, 07--B divider output, 08--C divider output, 09--D divider output, 10--connection of positive feed voltage $+U_{cc}$, 11--CV input, 12--TT oscillator input, 13--DC output, 15--inverting IST input, 16--A divider input, 17--B divider input, 18--C divider input. Schematic diagram and wiring of outlets is shown in Figure 26.

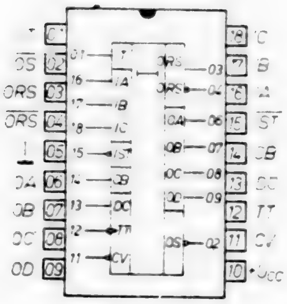


Figure 26. Schematic diagram and wiring of outlets of integrated circuits D355D, E355D

The ratio of division for connection with circuits D355D, E355D from TT oscillator input to OA output is 1024, for OB output the input voltage is min. -0.8 V, max. +7.25 V (except inputs TT and CV), input voltage of TT and CV inputs is min. -0.5 V, max. +U_{cc} + 0.5 V, output voltage min. -0.5 V, max. +8 V (except inverting ORS relay input which can have a max. voltage of +14.5 V), power dissipation max. 400 mW. Similarly to the preceding parts, the D355D is designed for operation in the temperature range of approximately 0°C to +70°C, the E355D from -25°C to +85°C.

Recommended operational values: feed voltage 4.75 V to 7.25 V, input voltage at level L max. 0.8 V, at level H min. 2.4 V. Output current of inverting ORS output at level L max. 50 mA. The trigger pulse width must be min. 20 μs, width of the alignment pulse min. 200 μs. Informative operational values: output voltage at level L of OA output max. 0.4 V at output current of 20 mA, of outputs OB, oc, od, os and ORS max. 0.4 V at current of 4 mA, inverting ORS relay output max. 0.5 V at current 50 mA, of DC output max. 0.2 V at current of 10 mA. Highest operational frequency is 105 kHz.

BCD Code Converters D345D Through D348D

The bipolar integrated circuits D345D through D348D are produced by the injection logic technique I^2L by the Semiconductor Plant in Frankfurt/O. They are intended for application as converters of input information in BCD code into output information with a 7-element image display with luminous diodes. Input stages of the circuits are compatible with log. circuits TTL and LS TTL. Output stages take the form of circuits with constant current which are preset in types D345D and D347D and can be controlled in types D346D and D348D by means of external resistance or regulator. The wiring of outlets of circuits D345D and D347D is shown in Figure 27, that of circuits D346D and D348D in Figure 28.

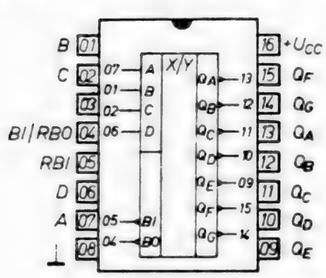


Figure 27. Schematic diagram and wiring of outlets of integrated circuits D345D, D347D

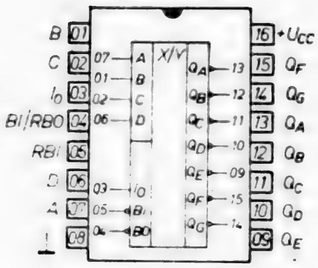


Figure 28. Schematic diagram and wiring of outlets of integrated circuits D346D, D348D

With the exception of outlet 03--which is not in the first two types and in the other two serves to control their output current--both outlet connections coincide with the wiring of converters D146D, D147D (SN7446, SN7447). In connection with 7-element displays with luminous diodes, new more modern circuits can replace the older types D146D, D147D.

Limiting values (for all types): feed voltage min. 0 V, max. 7 V, output voltage of outputs Q_A through Q_G min. 0 V, max. +7.5 V, total power dissipation in D345D, D347D at input current of max. 18 mA is permissible to a max. of 400 mW, in D346D, D348D at current of 30 mA max. 1020 mW (can be loaded in static operation by output current of only max. 20 mA). Permissible range of operational temperatures approximately 0°C to +70°C. Characteristic static values appear in Table 11, functional table of converters D345D, D346D in Table 12, of converters D347D, D348D in Table 13.

Table 11. Characteristic values of D345D Through D348D Apply at ϑ_a = 0°C through +70°C

			min.—max.	
Power input				
U_{CC} = 5,25 V	D345D, D347D	I_{CC}	≤20	mA
U_{CC} = 5,25 V, I_{OL} = 20 mA,	D346D, D348D	I_{CC}	≤35	mA
U_{CC} = 5,25 V, I_{OL} = 40 mA, U_{OL} = 4 V	D346D, D348D	I_{CC}	≤50	mA
Input voltage--level H				
U_{CC} = 4,75 V		U_{IH}	≥2	V
Input voltage--level L				
U_{CC} = 4,75 V		U_{IL}	≤0,8	V
Output voltage--level H				
U_{CC} = 4,75 V, I_{OH} = 20 μA,	Q_A až Q_G	U_{OH}	≥7,5	V
Output voltage--level L				
U_{CC} = 4,75 V, I_{OL} = 8 mA,	RBO/BI	U_{OL}	≤0,4	V
Output voltage--level H				
U_{CC} = 5,25 V, I_{OH} = 250 μA,	RBO/BI	U_{OH}	≥ 2,4	V
Input current--level L				
U_{CC} = 5,25 V, U_{IL} = 0,4 V		$-I_{IL}$	≤400	μA
Input current--level H				
U_{CC} = 5,25 V, except input BI/RBO		I_{IH}	≤20	μA
Output current--level L outputs Q_A to Q_G				
U_{CC} = 5,25 V, U_{OL} = 4 V	D345D, D347D	I_{OL}	8 až 13	mA
	D346D, D348D[1])	I_{OL}	0 až 20	mA

1) Output current can be adjusted with a view to the permissible power dissipation and maximum ambient temperature (see limiting values) to a value of up to 40 mA.

Table 12. Functional table for code converters D345D, D346D

Decadic number or function	Inputs						Outputs						
	RBI	*A*	*B*	*C*	*D*	*BI/RBO*	Q_A	Q_B	Q_C	Q_D	Q_E	Q_F	Q_G
0	H	H	L	L	L	H	L	L	L	L	L	L	H
1	X	H	L	L	L	H	H	L	L	H	H	H	H
2	X	L	H	L	L	H	L	L	H	L	L	H	L
3	X	H	H	L	L	H	L	L	L	L	H	H	L
4	X	L	L	H	L	H	H	L	L	H	H	L	L
5	X	H	L	H	L	H	L	H	L	L	H	L	L
6	X	L	H	H	L	H	L	H	L	L	L	L	L
7	X	H	H	H	L	H	L	L	L	H	H	L	H
8	X	L	L	L	H	H	L	L	L	L	L	L	L
9	X	H	L	L	H	H	L	L	L	L	H	L	L
10	X	L	H	L	H	H	L	L	L	H	L	L	L
11	X	H	H	L	H	H	H	H	L	L	L	L	L
12	X	L	L	H	H	H	L	H	H	L	L	L	H
13	X	H	L	H	H	H	H	L	L	L	L	H	L
14	X	L	H	H	H	H	L	H	H	L	L	L	L
15	X	H	H	H	H	H	L	H	H	H	L	L	L
BI	X	X	X	X	X	L	H	H	H	H	H	H	H
RBI	L	L	L	L	L	L	H	H	H	H	H	H	H

Table 13. Functional table for code converters D347D, D348D

Decadic number or function	Inputs						Outputs						
	RBI	*A*	*B*	*C*	*D*	*BI/RBO*	Q_A	Q_B	Q_C	Q_D	Q_E	Q_F	Q_G
0	H	L	L	L	L	H	L	L	L	L	L	L	H
1	X	H	L	L	L	H	H	L	L	H	H	H	H
2	X	L	H	L	L	H	L	L	H	L	L	H	L
3	X	H	H	L	L	H	L	L	L	L	H	H	L
4	X	L	L	H	L	H	H	L	L	H	H	L	L
5	X	H	L	H	L	H	L	H	L	L	H	L	L
6	X	L	H	H	L	H	L	H	L	L	L	L	L
7	X	H	H	H	L	H	L	L	L	H	H	L	H
8	X	L	L	L	H	H	L	L	L	L	L	L	L
9	X	H	L	L	H	H	L	L	L	L	H	L	L
10	X	L	H	L	H	H	H	H	H	H	H	H	L
11	X	H	H	L	H	H	L	H	H	L	L	L	L
12	X	L	L	H	H	H	H	L	L	L	L	L	H
13	X	H	L	H	H	H	H	L	L	L	L	H	L
14	X	L	H	H	H	H	H	H	H	L	L	H	L
15	X	H	H	H	H	H	L	L	L	H	L	L	L
BI	X	X	X	X	X	L	H	H	H	H	H	H	H
RBI	L	L	L	L	L	L	H	H	H	H	H	H	H

Excitation Circuit E412D

The integrated circuit E412D is a logical and coupling circuit resistant to short-circuiting which combines three logic members AND (two with 4, one with 3 inputs and a common third state input with 3-state outputs). The part is characterized by high resistance to interference and a wide range of feed voltage. It is suited for applications as an excitation circuit

for processor units in industrial electronics. The circuit's logic functions: if a signal of level L is on the control input of third state T, then it applies that

$$Y_1 = A_1 \cdot B_1 \cdot \bar{D}_1$$

$$Y_2 = A_2 \cdot B_2 \cdot \bar{D}_2$$

$$Y_3 = A_3 \cdot \bar{D}_3$$

If signal of level H is on input T then applies that

$$Y_1 = Y_2 = Y_3 = \text{third state}$$

The functional schematic diagram of the integrated circuit together with wiring of outlets is shown in Figure 29. The part is contained in a DIL plastic case of the type 21.2.1.2.18 with 2x nine outlets in two rows.

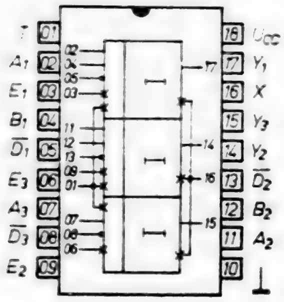


Figure 29. Schematic diagram and wiring of outlets of integrated circuit E412D

The function of individual outlets: 01--control input of third state T, 02--input A_1, 03--outlet E_1, 04--input B_1, 05--inverting input D_1, 06--outlet E_3, 07--input A_3, 08--inverting input D_3, 09--outlet E_2, 10--grounding outlet, 11--input A_2, 12--input B_2, 13--inverting input D_2, 14--output Y_2, 15--output Y_3, 16--input X, 17--output Y_1, 18--feed voltage $+U_{cc}$.

The E412D integrated circuit can be fed by a wide range of voltages from 0 V to 35 V. The limiting and characteristic values of the circuit are shown in Table 14. The recommended values of feed voltage are typified by voltages of 32, 24 and 14 V. With them are listed static values, dynamic values only for the 24 V voltage. The input outlet X is common to all three logic members and is used for limiting. It can be used to set on the outputs of all the three logic members the level H. Inputs E serve to set the basic delay time of the individual logic members. Input T can be used to set the outputs of all three members into the third state.

Recommended operational conditions: feed voltage 14 to 32 V, input voltage of inputs A, B and D at level L within -0.15 V to +5 V, in level H 7.5 V to 44 V, input current of inputs A, B and D with protective input resistance of 5.6 kΩ within -5.0 V to +44 V, voltage of outlet X max. 30 V, voltage of outlet T at level L max. 0.8 V, at level H 2.0 V, logic gain N_0 max. 20 (whereby $N_0 = 1$ corresponds to I = 0.3 mA).

Table 14. Electrical Magnitude Values of the E412D Excitation Circuit

Limiting values		min.	max.	
Feed voltage	U_{CC}	•	35	V
Limiting voltage (outlet 16)	U_K	•	35	V
Input volatge on inputs A, B, D	$U_{I\,A,B,D}$	—0,15	44	V
Input voltage on outlet T[1])	U_{IT}	—0,15	5,5	V
Input voltage ahead of prot. resistance 5.6 kΩ on inputs A, B, D				
permanent	U_I	—30	+50	V
$t \le 6$ μs, $f \le 300$ Hz	U_{IM}	—300	+300	V
$t \le 12$ μs, $f \le 300$ Hz	U_{IM}	—150	+150	V
Output voltage on output Y ahead of protective resistance 560 Ω				
$t \le 6$ μs, $f \le 300$ Hz	U_O	—300	+300	V
$t \le 12$ μs, $f \le 300$ Hz	U_O	—150	+150	V
Voltage on input E				
$U_I = U_O \ge -0{,}15$ V	U_{IE}	0,15	6,0[2])	V
U_I and $U_O \le -0{,}15$ V ahead of protective resistance	U_{IE}	no voltage permitted		
Thermal resistance trans./ambience	R_{thja}		80	K/W
Transition temperature	ϑ_j		125	°C
Total power dissipation at $\vartheta_a \le 37$ °C	P_{tot}		1,1	W
$\vartheta_a = 85$ °C	P_{tot}		0,5	W
Range of ambient operational temperatures	ϑ_a	—10	+85	°C

Characteristic Static Values:		min.—max.	
Power input $U_{CC} = 32$ V	I_{CC}	≤12	mA
Input current - level L $U_{CC} = 24$ V, $U_{IL} = 5$ V	I_{IL}	0,1 to 0,3	mA
Input current - level H $U_{CC} = 24$ V, $U_{IH} = 32$ V	I_{IH}	0,1 to 0,3	mA
Output voltage - level H $U_{CC} = 14$ V, $-I_{OH} = 6$ mA, $U_{IH} = 7{,}5$ V on A, B, $U_{IL} = 5$ V on D, $U_{IT} = 0{,}8$ V	U_{OH}	≥11	V
Output voltage - level L $U_{CC} = 32$ V, $I_{OL} = 3{,}2$ mA, $U_{IH} = 7{,}5$ V on A, B, D, $U_{IT} = 0{,}8$ V	U_{OL}	≤0,5	V
Control current from outlet X $U_{CC} = 32$ V, $U_{IH} = 7{,}5$ V on A, B, $U_{IL} = 5$ V on D, $U_X = 5$ V, $U_{IT} = 0{,}8$ V	$-I_X$	≤2	mA
Short-circuit current against ground - output at level H $U_{CC} = 32$ V, $U_{IH} = 7{,}5$ V on A, B, $U_{IL} = 5$ V on D, $U_{IT} = 0{,}8$ V	$-I_{OSH}$	≤22	mA
Current into outlet T $U_{CC} = 24$ V, $U_{IT} = 5{,}5$ V	I_{IT}	≤40	μA
Current from outlet T $U_{CC} = 24$ V, $U_{IT} = 0{,}4$ V	$-I_{IT}$	≤40	μA
Current into outlet Y in third state $U_{CC} = 32$ V, $U_O = 32$ V, $U_{IH} = 7{,}5$ V on A, B, D, $U_{IT} = 2{,}0$ V	I_O	≤50	μA
Current from outlet Y in third state $U_{CC} = 32$ V, $U_O = 0$ V, $U_{IH} = 7{,}5$ V on A, B, $U_{IL} = 5$ V on D, $U_{IT} = 2{,}0$ V	$-I_O$	≤25	μA
Dynamic values: = 25°C -5K			
Signal delay time of gates 1 and 3, on E condenser output $U_{CC} = 24$ V, $C_2 = C_6 = 33$ nF, $U_{IH} = 7{,}5$ V on A, B, $U_{IT} = 0{,}8$ V	t_{PLH1}	5,5 to 12	ms
	t_{PHL1}	1,5 to 4	ms
Signal delay time of gate 2 outlet E free $U_{CC} = 24$ V, $U_{IH} = 7{,}5$ V on A, B, $U_{IT} = 0{,}8$ V	t_{PLH2}	2 to 9	μs
	t_{PHL2}	1 to 5	μs
Third state delay time of gate 1 $U_{CC} = 24$ V, $U_{IH} = 7{,}5$ V on A, B, D	t_{LZ}	≤1	μs
	t_{ZL}	≤1	μs
$U_{CC} = 24$ V, $U_{IH} = 7{,}5$ V on A, B	t_{HZ}	≤1	μs
	t_{ZH}	≤1	μs

Notes to Table 14:

1) Voltage U_{IT} can exceed 5.5 V, provided current is limited into input T on $I_{IT} \leqq 3$ mA.

2) Voltage on outlet E can be increased up to $U_{IE} = 8$ V, provided current is limited into outlet E to $I_E \leqq 0.5$ mA.

t) Short-circuit on outputs against feed voltage or against ground potential is permitted, provided that $P_{tot\ max}$ is not exceeded.

Schottky TTL Logic Integrated Circuits With Small Power Input DL000D to DL074D

The production enterprise Semiconductor Plants Frankfurt/O. is expanding the produced assortment of logic circuits by a new series of 11 types of Schottky TTL logical circuits with a low power input. The series includes all basic circuits for construction of economical computation devices with low power consumption. The parts offered for the time being are:

DL000D--4x logic members NAND with 2 inputs (variant SN74LS00N),

DL002D--4x logic members NOR with 2 inputs (SN74LS02D),

DL003D--4x logic members NOR with 2 inputs and open collector (SN74LS03N),

DL004D--6x inverters (SN74LS04N),

DL008D--4x logic members AND with 2 inputs (SN74LS08N),

DL010D--3x logic members NAND with 3 inputs (SN74LS10N),

DL011D--3x logic members AND with 3 inputs (SN74LS11N),

DL020D--2x logic members NAND with 4 inputs (SN74LS20N),

DL021D--2x logic members AND with 4 inputs (SN74LS21N),

DL030D--logic member NAND with 8 inputs (SN74LS30N),

DL074D--pair of flip-flop circuits D with inputs S (setting) and R (zero setting) actuated by L-H pulse edge, i.e., information on input D is transmitted by pulse to output Q (SN74LS74N).

These integrated circuits are produced by the Schottky TTL integrated circuit technology. They are contained in plastic DIL casings with 2x seven outlets. The wiring of outlets together with the schematic diagram of individual types is shown in Figure 30.

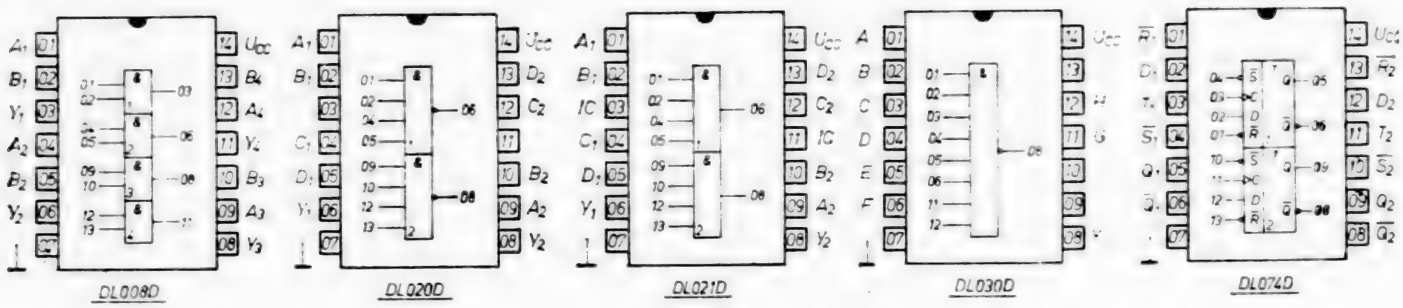


Figure 30. Schematic diagram and wiring of outlets of Schottky TTL logical integrated circuits with low power input DL008D through DL074D

Limiting values of logic members: feed voltage 0 V to +7.0 V, input voltage on diode input U_I max. 7.0 V, input voltage of emitter inputs max. 5.5 V (at current I_{IH} max. 1 mA), input voltage between two inputs of circuits with multi-emitter inputs max. 5.5 V (at I_{IH} max. 1 mA), output voltage at level H in circuits with open collector circuit max. 7.0 V, output voltage at level H on 3-state outputs at high impedance max. 5.5 V, range of ambient operational temperatures 0°C to +70°C. Recommended operational values and characteristic values are shown in Table 15.

Table 15. Characteristic values of Schottky TTL integrated circuits of the DL000D through DL074D series with low power input

Characteristic values: δ_α = 0°C to +70°C				min.—max.	
Input voltage - level H			U_{IH}	≥2,0	V
Input voltage - level L			U_{IL}	≤0,8	V
Input interception voltage	U_{CC} = 4,75 V, I_I = —18 mA		$-U_D$	≤1,5	V
Output voltage - level H	U_{CC} = 4,75 V, U_{IL} = 0,6 V, U_{IH} = 2,0 V, I_{OH} = —400 µA		U_{OH}	≥2,7	V
Output voltage - level L	U_{CC} = 4,75 V, U_{IH} = 2,0 V, U_{IL} = 0,8 V				
	I_{OL} = 8 mA		U_{OL}	≤0,5	V
	I_{OL} = 4 mA		U_{OL}	≤0,4	V
Input current - level H	U_{CC} = 5,25 V, U_{IH} = 2,7 V		I_{IH}	≤20	µA
	U_{CC} = 5,25 V, U_{IH} = 7,0 V		I_{IH}	≤100	µA
Output current - level H	U_{CC} = 4,75 V, U_{OH} = 5,5 V, U_{IL} = 0,8 V	DL003D	I_{OH}	≤100	µA
Data applies to gates:					
Input current - level L	U_{CC} = 5,25 V, U_{IL} = 0,4 V		$-I_{IL}$	≤400	µA
Power input of one log. member - level H	U_{CC} = 5,25 V, U_{IL} = 0 V		I_{CCH}	≤0,4	mA
Power input of one log. member - level L	U_{CC} = 5,25 V, U_{IH} = 4,5 V		I_{CCL}	≤1,1	mA
Dynamic values of gates:	U_{CC} = 5,0 V, ϑ_a = 25°C, C_L = 15 pF, R_L = 2 kΩ				
Delay time for signal passage during transition of output from level L to H			t_{PLH}	≤15	ns
level H to L			t_{PHL}	≤15	ns
level L to H		DL003D	t_{PLH}	≤32	ns
level H to L		DL003D	t_{PHL}	≤28	ns
level H to L		DL030D	t_{PHL}	≤20	ns
Flip-flop circuit DL074D:					
Input current - level H	U_{CC} = 5,25 V, U_{IH} = 2,7 V, input D, T	$I_{IH(D)}$,	$I_{IH(T)}$	≤20	µA
	U_{CC} = 5,25 V, U_{IH} = 7,0 V, input D, T	$I_{IH(D)}$,	$I_{IH(T)}$	≤100	µA
	U_{CC} = 5,25 V, U_{IH} = 2,7 V, input R, S	$I_{IH(R)}$,	$I_{IH(S)}$	≤40	µA
	U_{CC} = 5,25 V, U_{IH} = 7,0 V, input R, S	$I_{IH(R)}$,	$I_{IH(S)}$	≤200	µA
Input current - level L	U_{CC} = 5,25 V, U_I = 0,4 V, input D, T	$I_{IL(D)}$,	$I_{IL(T)}$	≤0,4	mA
	input R, S	$I_{IL(R)}$,	$I_{IL(S)}$	≤0,8	mA
Output short-circuit current [1]	U_{CC} = 5,25 V, $t \le 1$ s	$-I_{OS}$		20 to 100	mA
Power input of the entire circuit	U_{CC} = 5,25 V, input T grounded, all outputs open	I_{CC}		≤8	mA
Dynamic values:	U_{CC} = 5 V, ϑ_a = 25 °C, C_L = 15 pF R_L = 2 kΩ				
Signal delay time during transition of output from level L to H		t_{PLH}		≤25	ns
level H to L		t_{PHL}		≤40	ns

1) Only one output can be short-circuited.

All types of integrated circuits of the DL000D series are fed with a voltage of 5.0 V which must be maintained with a precision of ± 0.25 V. Maximum logic gain of each member permitted at level L is 10, at level H max. 20, whereby gain of output 1 corresponds to a current of 1.6 mA. Logic functions of circuits, as well as wiring of outlets, coincide with those of analogous types of the most widely used conventional logical circuits TTL of the SN74 series (MH74). Functional table of the DL074D flip-flop circuit is shown in Table 16.

Table 16. Functional table of the DL074D flip-flop circuit

Inputs				Outputs	
S	*R*	*T*	*D*	*Q*	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H[1])	H[1])
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q_0}$

[1]) Unstable state
↑ Switching pulse edge L-H
X Random state (level H or L)

[No 6, Jun 1983 pp 217-219]

[Excerpts] [Part 5] The U825G Integrated Circuit for Calculators

The U825G integrated circuit (produced by CMOS technology) is designed for application in pocket calculators, where it performs the function of a circuit for computation of the subsequently specified mathematical functions, a timing circuit cooperating with a liquid crystal display. The computation part of the circuit performs the following mathematical functions:

--addition, subtraction, multiplication, division, percentages, roots;

--operations with constants and chain operations;

--uses its own memory;

--addition and subtraction of values in memory;

--the extent of computations can be up to 10^7, eventually $10^8 - 1$;

--displays a floating decimal comma.

The timing part of the integrated circuit performs the following functions:

--the time base operates with a quartz crystal;

--time display in 12 h cycles, display of date, day of the week, hours and minutes;

--potential for separate setting of all parts of time indication;

--built-in piezoelectric alarm can be set independently;

--a part of the timing circuit is formed by a stopwatch, the functioning of which is fully independent of the timing part--it operates for up to 9 h 59 min 59 sec with display accuracy of 0.1 sec.

The integrated circuit indicates an erroneous entry due to an impermissible or undefined operation. At the same time it suppresses zero figures ahead of the digital entry.

The U825G integrated circuit is built into a flat plastic casing measuring 20 x 14 x 2 mm with wire outlets on all four sides. Wiring of outlets and schematical diagram of the circuit are shown in Figure 38. Limiting and characteristic values of the circuit are listed in Table 23.

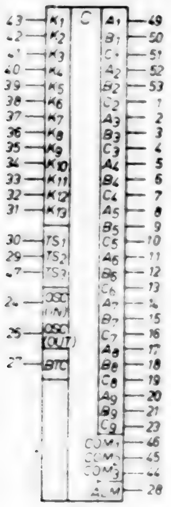


Figure 38. Schematic diagram and wiring of outlets of the U825G integrated circuit

Table 23. Limiting and characteristic values of the U825G integrated circuit

Limiting values: $\vartheta_a = 0$ °C až +40 °C				
		min.	max.	
Feed voltage re U_{SS}	U_{DD}	—3,5	+0,3	V
Input voltage	U_I	U_{DD}	+0,3	V
Ambient operational temperature range	ϑ_a	0	+40	°C
Range of storage temperatures	ϑ_{stg}	—55	+125	°C
Characteristic values: $\vartheta_a = 25$ °C				
Power input w/clock running			min.—max.	
$U_{DD} = -3$ V, $f_{osc} = 30{,}72$ kHz,				
all switches on	I_{DD}		≤17	µA
Output voltage - level H				
outputs COM_1 to COM_3, A_1 to A_9,				
B_1 to B_9, C_1 to C_9	U_{OH}	2/3 U_{DD} + 0,2 to 2/3 U_{DD} — 0,2		V
	U_{OH}	U_{DD} + 0,2 to U_{DD}		
outputs K_1 to K_7, K_{10} to K_{13}, ALM	U_{OH}	U_{DD} + 0,2 to U_{DD}		V
Output voltage - level L				
outputs COM_1 to COM_3, A_1 to A_9,				
B_1 to B_9, C_1 to C_9	U_{OL}	1/3 U_{DD} + 0,2 to 1/3 U_{DD} — 0,2		V
	U_{OL}	0 to	—0,2	V
outputs K_1 K_7, K_{10} to K_{13}, ALM	U_{OL}	0 to	—0,2	V
Delay time	t_D		~ 3,125	ms
Duration of clock/alarm contact break				
with switches S_1 or S_2 open	$t_{OFF\ S_1,\ S_2}$		≤3,125	ms
Duration of connection in actuating contact				
of keyboard 1	t_{SS}		≤6,250	ms
Duration of break in switch S_1 cut-off	$t_{OFF\ S}$		≤21,875	ms

The recommended operational wiring of the calculator circuit using the U825G circuit as shown in Figure 39 applies at the following values:

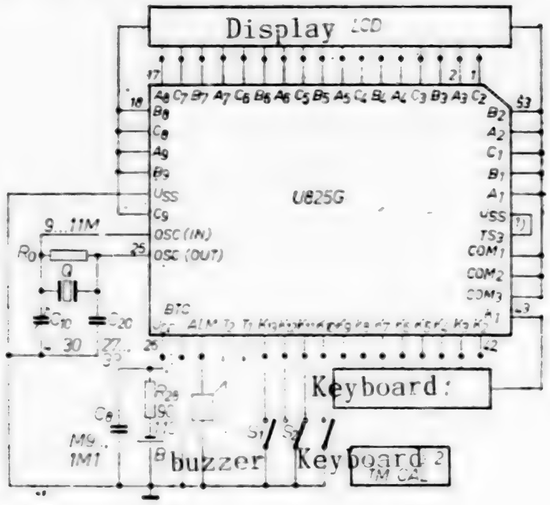


Figure 39. Recommended operational wiring of U825G circuit in the calculator

Negative feed voltage

U_{DD}	-3.2 to -2.8	V

Feed voltage

U_{SS}	0	V

Resistance of connected keyboard contacts

R_{Kg}	$\leqq 100$	kΩ

Oscillator frequency

f_{osc}	30.72	kHz

Resistance of disconnected keyboard contacts

R_{k}	$\leqq 1600$	kΩ

Input voltage - level H

outlets K_4 to K_{13}

U_{IH}	$-U_{DD} + 0.5$ to $-U_{DD}$	V

Input voltage - level L

outputs K_4 to K_{13}

U_{IL}	0 to +05	V

Alarm frequency

f_S	3.84	kHz

Buzzer capacity

C_S	$\leqq 25$	pF

U826G Integrated Circuit for Calculators

The U826G integrated circuit is a special CMOS LSI circuit for application in battery-powered pocket calculators for scientific and technical uses. The circuit combines an internal oscillator and a time frequency generator, an internal decoder of the keyboard and disconnecting of its contacts, automatic zero setting when the calculator is turned on, error indicator for impermissible or undefined operations, complementary output exciter for direct excitation of display with liquid crystals with special symbols as well as an independent memory.

The integrated circuit can display an 8-digit mantissa, 2-digit exponents and special mantissa and exponent signs. The schematic diagram together with wiring of outlets are shown in Figure 40. The circuit comes in a special flat plastic casing with 56 ribbon outlets distributed along all four sides. Casing dimensions (without outlets) are 20 x 14 mm, maximum thickness is 2 mm. The U826G circuit is an equivalent of the international type T3636.

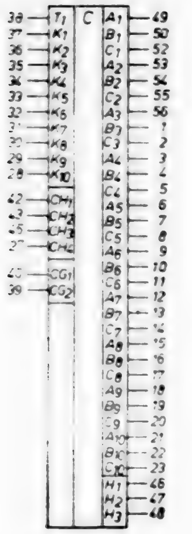


Figure 40. Schematic diagram and wiring of outlets of the U826G integrated circuit

The U826G integrated circuit can perform the following mathematical functions:

--addition, subtraction, multiplication and division;

--memory operations (addition, substitution, storing into memory, reading from memory, zero setting);

--trigonometric functions (sine, cosine, tangent);

--inverse trigonometric functions (arcsin, arccos, arctan);

--hyperbolic trigonometric functions (sinh, cosh, tanh);

--logarithmic functions (ln, lx);

--raising to a power (x^2, e^x, 10^x, y^x);

--square and cube root;

--facultative calculus (x !);

--reciprocal functions (1/x);

--conversion of decadic degrees into degrees, minutes and seconds of arc and vice versa (DEG / DMS);

--conversion of polar coordinates into Cartesian coordinates and vice versa ($\rightarrow$ xy, $\rightarrow r\vartheta$);

--computation in brackets at two levels;

--percentual functions (Δ %);

--computations with a constant;

--statistical functions ($n, \Sigma x, \Sigma x^2, \bar{x}, \sigma_{n-1}, \sigma_n$, DATA, DEL).

Functions of individual outlets: 1 through 23, 46 through 50, 52 through 56--outputs for control of display with liquid crystals (A_1 through A_{10}, B_1 through B_{10}, C_1 through C_{10}, H_1 through H_3); 24, 51--grounding points (U_{SS}); 25, 26, 44--not covered (NC); 27, 42, 43, 45--measuring points (CH_1 through CH_4); 28 through 38--keyboard connection (K_1 through K_{10}, T_1); 39, 40--oscillator outlets (CG_1, CG_2); 41--negative feed voltage connection (U_{DD}).

Limiting values of the U826G circuit: feed voltage U_{DD} min. -3.5 V, max. +0.3 V, input voltage min. U_{DD}, max. +0.3 V (both voltages in relation to zero potential U_{SS}). Range of permissible ambient temperatures 0°C to +40°C. Characteristic values are shown in Table 24.

Table 24. Characteristic values of the U826G integrated circuit; applicable at $\delta_c = 25°C$

			min. —max.	
Power input		I_{DD}	≤ 160	μA
Output voltage - level $H^{1)}$		U_{OH}	$U_{DD} + 0{,}2$ to U_{DD}	V
Output voltage - level $L^{1)}$		U_{OL}	U_{SS} to $U_{SS} - 0{,}2$	V
Output voltage - level H		U_{OH_1} 2)	$2/3\ U_{DD} + 0{,}2$ to $2/3\ U_{DD} - 0{,}2$	V
		U_{OH_2} 3)	$U_{DD} + 0{,}2$ to U_{DD}	V
Output voltage - level L		U_{OL_2} 2)	$1/3\ U_{DD} + 0{,}2$ to $1/3\ U_{DD} - 0{,}2$	V
		U_{OL_1} 3)	U_{SS} to $U_{SS} - 0{,}2$	V
Output resistance - level L				
	$U_O = U_{SS} - 0{,}5$ V	R_{OL} 1)	≤ 5	kΩ
	$U_O = U_{SS} - 0{,}5$ V	R_{OL} 2)	≤ 200	kΩ
	$U_O = 1/3\ U_{DD} - 0{,}5$ V, $U_O = U_{SS} - 0{,}5$ V	R_{OL} 3)	≤ 100	kΩ
Output resistance - level H				
	$U_O = U_{DD} + 0{,}5$ V	R_{OH} 2)	≤ 200	kΩ
	$U_O = 2/3\ U_{DD} + 0{,}5$ V, $U_O = U_{DD} + 0{,}5$ V	R_{OH} 3)	≤ 100	kΩ
Operational frequency of oscillator	$R_1 = 120\ \Omega$	f_{osc}	56 to 80	Hz
Typical speed of computations		t_R	0,1 to 2,7	s

1) Measured at input/output of keyboard
2) Measured at output of segments A_1 to A_{10}, B_1 to B_{10}, C_1 to C_{10})
3) Measured at output of plate (H_1, H_2, H_3)

An example of recommended wiring of the U826G integrated circuit in connection with liquid crystals display and pushbutton keyboard is shown in Figure 41. The recommended operational conditions for the same wiring are shown in Table 25. Potential combinations of individual mathematical functions are shown in Table 26.

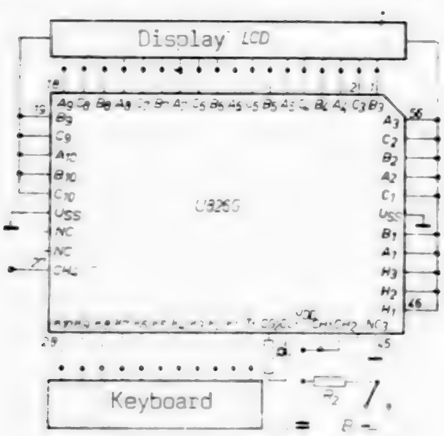


Figure 41. Recommended operational wiring of the U826G circuit in a calculator

Table 25. Recommended operational values for the U826G integrated circuit

		nomin.	min.—max.	
Feed voltage [1]	U_{DD}	—3,0	—3,2 to —2,8	V
Input voltage - level H [1]	U_{IH}		U_{DD} to U_{DD} + 0,5	V
Input voltage - level L [1]	U_{IL}		—0,5 to 0	V
Insulation resistance of open contacts of pushbutton keyboard $U_T = 1/2\ U_{DD}$	R_{Koff}		≥1600	kΩ
Contact resistance of connected contacts of pushbutton keyboard	R_{Kon}		≤25	kΩ
Resistance	R_1	120	114 to 126	kΩ
	R_2	100	90 to 110	Ω
Condenser	C	1	0,8 to 1,2	μF
Ambient operational temperature	ϑ_a	25	0 to 40	°C

1) Related to U_{SS} = 0 V

Table 26. Potential combinations of computation functions of the U826G integrated circuit

B \ A	4 základní druhy výpočtů (1)	(2) Statistické funkce	(3) Závorky 1. úrovně	(4) Závorky 2. úrovně
(5) 4 základní druhy výpočtu	—	x	x	x
(6) paměťové funkce	x	0	x	x
$1/x$, x^2, $\sqrt{\ }$	x	x	x	x
ln, lg, e^x, 10^x	x	x	x	x
$\sqrt[3]{\ }$, y^x	x	x	x	x
sin, cos, tan	x	x	x	x
arcsin, arccos, arctan	x	x	x	x
sinh, cosh, tanh	x	x	x	x
$x!$	x	x	x	x
DEG/DMS	x	0	x	0
xy/rα	0	0	0	0
(7) statistické funkce	0	—	0	0
(8) závorky 1. a 2. úrovně	x	0	—	—

Computation of functions in column A with functions in line B is:
- x - possible,
- 0 - impossible

Key:

(1) 4 basic types of computations
(2) Statistical functions
(3) Brackets, 1st level
(4) Brackets, 2nd level
(5) 4 basic types of computations
(6) Memory functions
(7) Statistical functions
(8) 1st and 2nd level brackets

8-bit Processor Unit for the U830C Microcomputers

The integrated circuit U830C is an 8-bit processor unit (produced by silicon gate technology with conductivity N) for microcomputers. It is a developmental product of the Research and Technological Center for Microelectronics ZFTM in Dresden. It is characterized by the following properties:

--14-bit busbar control by microinstructions;

--a set of microinstructions contains 58 instructions (among others, for addition, subtraction, logical functions, carry-over, skip, formation of complements, increments, decreases, operations with individual bits, decimal corrections);

--input and output of data occurs along two congruent two-way channels K1 and K2;

--input and output of signal (N, Z, V, C) occurs through channel K3;

--the unit contains 18 internal registers;

--operation is asynchronous;

--the circuit is compatible with TTL logic, outputs can actuate one standardized TTL load;

--operation requires only one feed voltage of 5 V ± 5 percent;

--up to 4 integrated U830C circuits can be connected in cascade for expansion of the processed word.

The part comes in a ceramic DIL casing with 2 x 24 outlets in two rows. The wiring of outlets and logic diagram of the U830C integrated circuit is shown in Figure 42.

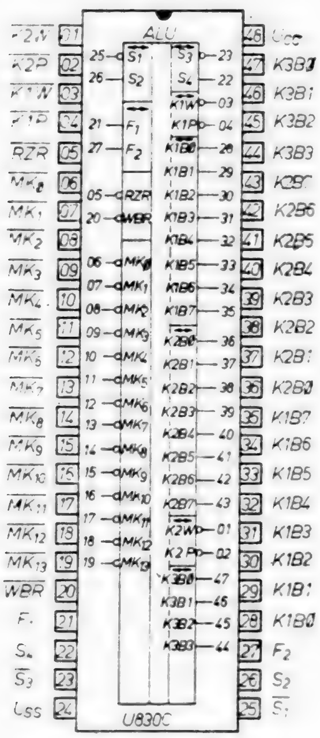


Figure 42. Schematic diagram and wiring of outlets of the U830C integrated circuit

Limiting values of the U830C circuit: feed voltage U_{CC}; input voltage U_I and output voltage U_0 can be min. -0.5 V and max. 7.0 V; power dissipation max. 1.8 W; range of ambient operational temperature 0°C to +70°C; range of storage temperatures -65°C to +150°C.

Characteristic values: feed voltage U_{CC} prescribed at 5 V $\pm$0.25 V; input voltage at level L is min. -0.5 V and max. 0.8 V, at level $\bar{H}$ min. 2 V and max. U_{CC}. Loading capacity C_L max. 100 pF. Output voltage at level L max. 0.4 V, at level H min. 2.4 V, power input max. 340 mA, input current at level L max. 10 μA and input capacity max. 10 pF.

Adapting Busbar Circuit for the U834C Microcomputers

Another developmental product of the ZFTM in Dresden is the U834C control circuit for adapting of peripheral units to the computation busbar of the SKR small computer. It is produced by the silicon gate technology with conductivity N. The integrated circuit is characterized by:

--programmable control of data flow between processor and peripheral unit (U834C as slave);

--control of data flow between memory and peripheral units (U834C as master);

--additional transfer of reports from peripheral units (requirements for interruption, DMA requirements) on processor;

--the U834D integrated circuit is programmable from the processor in 1,152 various functional variants;

--operational times are very short;

--operation is asynchronous;

--the circuit is compatible with TTL logic, outputs can actuate a standardized TTL load;

--operation of the circuit calls for only one feed voltage of 5 V $\pm$5 percent.

The integrated circuit comes in a DIL ceramic casing with 2 x 24 outlets in two rows. The wiring of outlets and a functional schematic diagram of the circuit are shown in Figure 43.

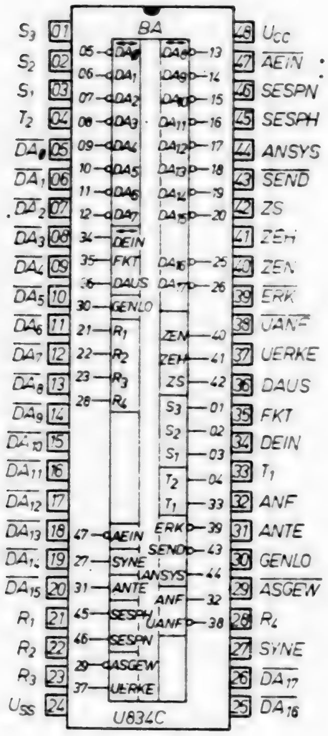


Figure 43. Schematic diagram and wiring of outlets of the U834C integrated circuit

Limiting values of the adapting circuit: feed voltage U_{CC}, input voltage U_I and output voltage U_O can be min. -0.5 V and max. 7.0 V; power dissipation max. 1.2 W; range of ambient operational temperatures 0°C to +70°C; range of storage temperatures -55°C to +155°C.

Characteristic values: feed voltage 5.0 V ± 0.25 V; input voltage at level L min. -0.5 V and max. 0.8 V; at level H min. 2 V and max. U_{CC}. Loading capacity max. 100 pF. Output voltage at level L max. 0.4 V, at level H min. 2.4 V. Power input max. 180 mA. Input voltage at level L max. 10 μA, input capacity max. 10 pF. Switching times: duration of time frequency period max. 2.5 μs (in master mode). Duration of time signal for reception t_{HI}ll (master data) is 560 ns, min. 120 ns; time signal duration till master data release 560 ns and min. 120 ns, time signal duration till ANSYS (data slave) average of 360 ns, min. 25 ns.

[No 7, Jul 1983 pp 251-253]

[Text] [Part 6] CMOS Logical Integrated Circuits

The series of CMOS logical integrated circuits--the first six types of which were initially produced a year ago by the Communications Plant (Funkwerk) Erfurt--is being expanded by the producer by additional nine new types. All come in a DIL plastic casing with 2 x 8 or 7 outlets in two rows. The new parts include the following types:

The D U4013D Bistable Flip-flop Circuit

Logical function: $Q(t_{n+1}) = D(t_n)$. The flip-flop circuits have separate timing, adjusting and zero setting inputs. Information fed to the data input D is transmitted in the flip-flop circuit with the positive edge of the clock pulse C to outputs Q and complementary Q. Data input during this state is blocked. The adjusting and zero setting inputs can be used to adjust the flip-flop circuit into state $(S = H \rightarrow Q) = H$ and set to zero $(R = H \rightarrow \bar{Q}) = H$. It is a variant of the international type CD4013.

The U4015D Double 4-Bit Shift Register

The circuit combines two 4-bit shift registers of the series-parallel converter type. Information from input D is stored by means of the leading edge of clock pulse C to point 1 of the shift register and is available at output O_{n4} (n = 1 or 2 system). With each additional leading edge of clock pulse C the information stored in the shift register is shifted to the next point. The contents of the register can be erased by means of the zero setting input R (outputs are in L level state). It is a variant of the CD4015 type.

The J-K U4027D Bistable Flip-flop Circuit

Both flip-flop circuits of the J-K master-slave type have independent clock and control inputs. Information fed to inputs J and K is transmitted to the circuit's "master" part with the trailing edge of the clock pulse. The "slave" part retains its own original information. With the leading edge of the clock pulse C the information is transmitted from the "master" part to the "slave" part and is available at outputs Q and complementary Q. The "master" part is simultaneously blocked for reception of data from inputs J and K. The adjusting and zero-setting inputs serve for adjusting $(S = H \rightarrow Q = H)$ and erasing $(R = H \rightarrow Q = H)$ of the flip-flop circuit. It is a variant of the CD4027 type.

The U4028D Converter of 8-4-2-1 BCD Code to Decadic Code

The U4028D integrated circuit contains a converter of the 8-4-2-1 BCD code to the code 1 of 10. An H level signal is available on a selected output while all the other outputs are at level L. It is a variant of the CD4028 type.

The U4035D 4-bit Shift Register With Synchronous Parallel Input

The circuit contains a 4-stage keyed series shift register with synchronously operating parallel inputs and one series input which control the first stage via logic of the flip-flop circuit J-K. When the excitation input P/S (parallel/series) is in state of level L, the register stages 2, 3 and 4 become connected in series arrangement into the flip-flop circuit D and operate in series. If the control input P/S is at level H, parallel inputs become connected to the register stages. In both types of operation the information is transmitted with the positive edge of the timing pulse.

If an H level signal is on the control input T/C (true/complement), the actual contents of the register will be available at outputs O_1 through O_4. If level L is at the T/C input, the register contents will be at outputs O_1 through O_4 in complementary form. The contents of all registers can be reset to zero simultaneously by means of input R (reset). Control functions of the T/C input are asynchronous with timing frequency. If inputs J and K of the register's first stage are mutually interconnected, the first stage will be connected to the flip-flop circuit D. It is a variation of the CD4035 type.

The U4042 D 4-bit Interception Register

Logic function: $Q(t_{n+1}) = D(t_n)$. The circuit combines four intermediate memories controlled by a common timing frequency. Information on data inputs is transmitted to outputs Q and complementary Q during the timing pulse level which is preset by input P (polarity). If the signal on input P is of level L, transmission of information at level L will occur on input C, at level H on input P or C. Outputs follow the input for as long as the leading edge of the timing frequency attains its highest level (at level L on input P) or the negative edge (at level H on input P) its lowest level. Information remains from there stored in the intermediate memory's flip-flop circuit. It is a variant of the CD4042 type.

Six U4050D Noninverting Excitation Stages

The integrated circuit combines in its overall system six noninverting stages. Logical function of each stage: 0 = 1. An input signal with a high H level can exceed the value of feed voltage U_{DD} if the integrated circuit is used as converter of logic levels. The part is suited for use as level converter COS/MOS to DTL/TTL. It can simultaneously excite two DTL/TTL loads. It is a variant of the CD4050 type.

Four U4093D Schmitt's Flip-flop Circuits

The circuit combines four logic members NAND with two inputs always followed by Schmitt's flip-flop circuit. Logic function: $O_1 = \overline{I_1 I_2}$. Logic members NAND switch positive and negative signals at various points. The difference between positive and negative switching voltage is defined as hysteresis voltage. It is a variant of the CD4093 type.

Six U40098D Inverters

The common system combines six inverters-exciters with 3-stage outputs. Logic function: O = I. The 3-stage outputs are controlled by two clearing inputs (CE_4, CE_2). Level H signal on input CE_4 causes four of the six inverters to change to a state of high impedance or a closed state depending on the input conditions. Similarly, level H signal on input CE_2 produces an analogous state in the remaining two inverters.

The limiting and characteristic values of the described CMOS integrated circuits U4013D through U40098D are listed in Table 27. Only in the case of the U4093D and U40098D is the limiting value of feed voltage U_{DD} given by the range of -0.5 V to +18 V; operational feed voltage can range between

3 to 15 V. Dynamic characteristic values of the U4013D through U4042D integrated circuits are shown in Table 28; they have not been determined for the remaining circuits as yet. Wiring of outlets and the functional schematic diagram of the individual types of integrated circuits are shown in Figure 44.

Table 27. Static limiting and characteristic values of the CMOS circuits U4013D through U4042D

Limiting Values:

		min.	max.	
Feed voltage	U_{DD}	U_{SS}—0,5	U_{SS}+20	V
U4093D, U400098D	D_{DD}	—0,5	+18	V
Input voltage	U_I	U_{SS}—0,5	U_{DD}+0,5	V
Output voltage	U_O	U_{SS}—0,5	U_{DD}+0,5	V
Power dissipation of each output transistor	P_T		100	mW
total	P_{tot}		300	mW
Loading capacity of output	C_L		5	nF
Range of ambient operational temperatures	ϑ_a	—25	+70	°C
Range of storage temperatures	ϑ_{stg}	—55	+125	°C

Characteristic Static Values:

Apply at U_{SS} = 0 V, ϑ_a = —25 °C to+70 °C, unless otherwise specified, U_I = U_{SS} or U_{DD}, $|I_O| \leq 1$ µA

			min.—max.	
Feed voltage		U_{DD}	3 to 18	V
	U4093D, U40098D	U_{DD}	3 to 15	V
Input voltage		U_I	0 to U_{DD}	V
Input voltage - level H	U_{DD} = 5 V	U_{IH}	≥3,5	V
	U_{DD} = 10 V	U_{IH}	≥7	V
	U_{DD} = 15 V	U_{IH}	≥11	V
Input voltage - level L	U_{DD} = 5 V	U_{IL}	≤1,5	V
	U_{DD} = 10 V	U_{IL}	≤3	V
	U_{DD} = 15 V	U_{IL}	≤4	V
Residual input current	U_I = U_{DD} = 18 V	I_{IH}	≤1	µA
	U_{DD} = 18 V, U_I = 0 V	$-I_{IL}$	≤1	µA
Output voltage - level L	U_{DD} = 5to 15 V	U_{OL}	≤0,05	V
Output voltage - level H	U_{DD} = 5 V	U_{OH}	≥4,95	V
	U_{DD} = 10 V	U_{OH}	≥9,95	V
	U_{DD} = 15 V	U_{OH}	≥14,95	V
Output current - level L	U_{DD} = 5 V, U_{OL} = 0,4 V	I_{OL}	≥0,4	mA
	U_{DD} = 10 V, U_{OL} = 0,5 V	I_{OL}	≥0,9	mA
	U_{DD} = 15 V, U_{OL} = 1,5 V	I_{OL}	≥2,4	mA
Output current - level H	U_{DD} = 5 V, U_{OH} = 4,6 V	$-I_{OH}$	≥0,4	mA
	U_{DD} = 10 V, U_{OH} = 9,5 V	$-I_{OH}$	≥0,9	mA
	U_{DD} = 15 V, U_{OH} = 13,5 V	$-I_{OH}$	≥2,4	mA
Input capacity		C_I	≤7,5	pF
Current input (static)	U_{DD} = 5 V U4013D, U4027D, U4042D	I_{DD}	≤30	µA
	U_{DD} = 10 V	I_{DD}	≤60	µA
	U_{DD} = 15 V	I_{DD}	≤120	µA
	U_{DD} = 5 V U4015D, U4028D, U4035D	I_{DD}	≤150	µA
	U_{DD} = 10 V	I_{DD}	≤300	µA
	U_{DD} = 15 V	I_{DD}	≤600	µA

Table 28. Characteristic dynamic values of CMOS integrated circuits U4013D through U4042D

[illegible] ϑ_a = 25 °C, U_{SS} = 0 V, C_L = 50 pF, U_I = U_{SS} … U_{DD}, $|I_O|$ ≤ 1 µA, t_r = t_f = 20 ns

	Typ		U4013D	U4015D	U4027D	U4028D	U4035D	U4042D	
1	**Doba nastavení dat**								
	U_{DD} = 5 V	t_{DS}	≥40	≥70	200	—	—	≥50	ns
	U_{DD} = 10 V	t_{DS}	≥20	≥40	≥75	—	—	≥30	ns
	U_{DD} = 15 V	t_{DS}	[illegible]	≥30	≥50			≥25	ns
2	**Doba nastavení vstupů J—K**								
	U_{DD} = 5 V	t_{SJK}	—	—	—	—	≥100	—	ns
	U_{DD} = 10 V	t_{SJK}	—	—	—	—	≥50	—	ns
	U_{DD} = 15 V	t_{SJK}	—	—	—	—	≥40	—	ns
3	**Doba nastavení paralelního vstupu**								
	U_{DD} = 5 V	t_{SP}	—	—	—	—	≥50	—	ns
	U_{DD} = 10 V	t_{SP}	—	—	—	—	≥30	—	ns
	U_{DD} = 15 V	t_{SP}	—	—	—	—	≥20	—	ns
4	**Šířka hodinového impulsu — úroveň H**								
	U_{DD} = 5 V	t_{CH}	≥140	—	≥140	—	≥200	≥200	ns
	U_{DD} = 10 V	t_{CH}	≥60	—	≥60	—	≥90	≥100	ns
	U_{DD} = 15 V	t_{CH}	≥40	—	≥40	—	≥60	≥60	ns
5	**Šířka hodinového impulsu — úroveň L**								
	U_{DD} = 5 V	t_{CL}	—	≥180	—	—	—	—	ns
	U_{DD} = 10 V	t_{CL}	—	≥80	—	—	—	—	ns
	U_{DD} = 15 V	t_{CL}	—	≥50	—	—	—	—	ns
6	**Doba náběhu a doběhu hodinových impulsů**								
	U_{DD} = 5 V	t_{Cr}, t_{Cf}	≤15	≤15	≤15	—	≤15	—	µs
	U_{DD} = 10 V	t_{Cr}, t_{Cf}	≤4	≤15	≤4	—	≤15	—	µs
	U_{DD} = 15 V	t_{Cr}, t_{Cf}	≤1	≤15	≤1	—	≤15	—	µs
7	**Kmitočet hodinových impulsů**								
	t_r = t_f = 5 ns								
	U_{DD} = 5 V	f_C	≤3,5	≤3	≤3,5	—	≤5	—	MHz
	U_{DD} = 10 V	f_C	≤8	≤6	≤8	—	≤12	—	MHz
	U_{DD} = 15 V	f_C	≤12	≤8,5	≤12	—	≤16	—	MHz
8	**Šířka nastavovacích a nulovacích impulsů**								
	U_{DD} = 5 V	t_{SH}, t_{RH}	≥180	—	≥180	—	t_{RH} ≥200	—	ns
	U_{DD} = 10 V	t_{SH}, t_{RH}	≥80	—	≥80	—	t_{RH} ≥90	—	ns
	U_{DD} = 15 V	t_{SH}, t_{RH}	≥50	—	≥50	—	t_{RH} ≥60	—	ns
9	**Šířka nulovacího impulsu**								
	U_{DD} = 5 V	t_{WRH}	—	≥200	—	—	—	—	ns
	U_{DD} = 10 V	t_{WRH}	—	≥80	—	—	—	—	ns
	U_{DD} = 15 V	t_{WRH}	—	≥60	—	—	—	—	ns
10	**Doba zpoždění ze vstupu** t_{DCHL}, t_{DCLH}, t_{DSLH}, t_{DRLH}								
	C to Q, $\overline{Q}$ / S to Q / R to $\overline{Q}$: U_{DD} = 5 V		≤300	—	≤300	—	—	—	ns
	U_{DD} = 10 V		≤130	—	≤130	—	—	—	ns
	U_{DD} = 15 V		≤90		≤90	—	—	—	ns
	S to $\overline{Q}$ / R to $\overline{Q}$: U_{DD} = 5 V	t_{DSHL}, t_{DSLH}	≤400	—	≤400	—	—	—	ns
	U_{DD} = 10 V	t_{DSHL}, t_{DSLH}	≤170	—	≤170	—	—	—	ns
	U_{DD} = 15 V	t_{DSHL}, t_{DSLH}	≤120	—	≤120	—	—	—	ns
11	**Doba přenosu hrany na Q a $\overline{Q}$, (O)**								
	U_{DD} = 5 V	t_{THL}, t_{TLH}	≤200	≤320	≤200	≤200	≤200	≤200	ns
	U_{DD} = 10 V	t_{THL}, t_{TLH}	≤100	≤160	≤100	≤100	≤100	≤100	ns
	U_{DD} = 15 V	t_{THL}, t_{TLH}	≤80	≤120	≤80	≤80	≤80	≤80	ns
12	**Doba zpoždění ze vstupu C na O_n**								
	U_{DD} = 5 V	t_{DHL}, t_{DLH}	—	≤320	—	—	≤300	—	ns
	U_{DD} = 10 V	t_{DHL}, t_{DLH}	—	≤160	—	—	≤200	—	ns
	U_{DD} = 15 V	t_{DHL}, t_{DLH}	—	≤120	—	—	≤160	—	ns
13	**Doba zpoždění ze vstupu R na O_n**								
	U_{DD} = 5 V	t_{DRHL}	—	≤400	—	—	≤300	—	ns
	U_{DD} = 10 V	t_{DRHL}		≤200	—	—	≤200	—	ns
	U_{DD} = 15 V	t_{DRHL}		≤160	—	—	≤160	—	ns
14	**Doba zpoždění ze vstupu I_n na O_m**								
	U_{DD} = 5 V	t_D	—	—	—	≤350	—	—	ns
	U_{DD} = 10 V	t_D	—	—	—	≤160	—	—	ns
	U_{DD} = 15 V	t_D	—	—	—	≤120	—	—	ns
15	**Doba zpoždění D_n na Q_n**								
	U_{DD} = 5 V	t_{DDQHL}, t_{DDQLH}	—	—	—	—	—	≤220	ns
	U_{DD} = 10 V	t_{DDQHL}, t_{DDQLH}	—	—	—	—	—	≤110	ns
	U_{DD} = 15 V	t_{DDQHL}, t_{DDQLH}	—	—	—	—	—	≤80	ns
16	**Doba zpoždění D_n na $\overline{Q}_n$**								
	U_{DD} = 5 V	$t_{DD\overline{Q}HL}$, $t_{DD\overline{Q}LH}$	—	—	—	—	—	≤300	ns
	U_{DD} = 10 V	$t_{DD\overline{Q}HL}$, $t_{DD\overline{Q}LH}$	—	—	—	—	—	≤150	ns
	U_{DD} = 15 V	$t_{DD\overline{Q}HL}$, $t_{DD\overline{Q}LH}$	—	—	—	—	—	≤100	ns
17	**Doba zpoždění C na Q**								
	U_{DD} = 5 V	t_{DCQHL}, t_{DCQLH}		—		—		≤450	ns
	U_{DD} = 10 V	t_{DCQHL}, t_{DCQLH}	—	—	—	—		≤[illegible]	ns
	U_{DD} = 15 V	t_{DCQHL}, t_{DCQLH}	—		—	—		160	ns
18	**Doba zpoždění C na $\overline{Q}$**								
	U_{DD} = 5 V	$t_{DC\overline{Q}HL}$, $t_{DC\overline{Q}LH}$		—			—	≤[illegible]	ns
	U_{DD} = 10 V	$t_{DC\overline{Q}HL}$, $t_{DC\overline{Q}LH}$	—	—			—	≤240	ns
	U_{DD} = 15 V	$t_{DC\overline{Q}HL}$, $t_{DC\overline{Q}LH}$	—			—		≤80	ns

Key to Table 28:

1. Data adjustment time
2. J-K inputs adjustment time
3. Parallel input adjustment time
4. Timing pulse width—level H
5. Timing pulse width--level L
6. Rise and decay times of timing pulses
7. Timing pulse frequency
8. Adjustment and zero-setting pulse width
9. Zero-setting pulse width
10. Delay time from input
11. Edge transmission time to Q and $\bar{Q}$, (O)
12. Delay time from input C to O
13. Delay time from input R to O^n
14. Delay time from input I_n to O_m
15. Delay time D_n to Q_n
16. Delay time D_n to $\bar{Q}_n$
17. Delay time C_n to Q_n
18. Delay time C to $\bar{Q}$

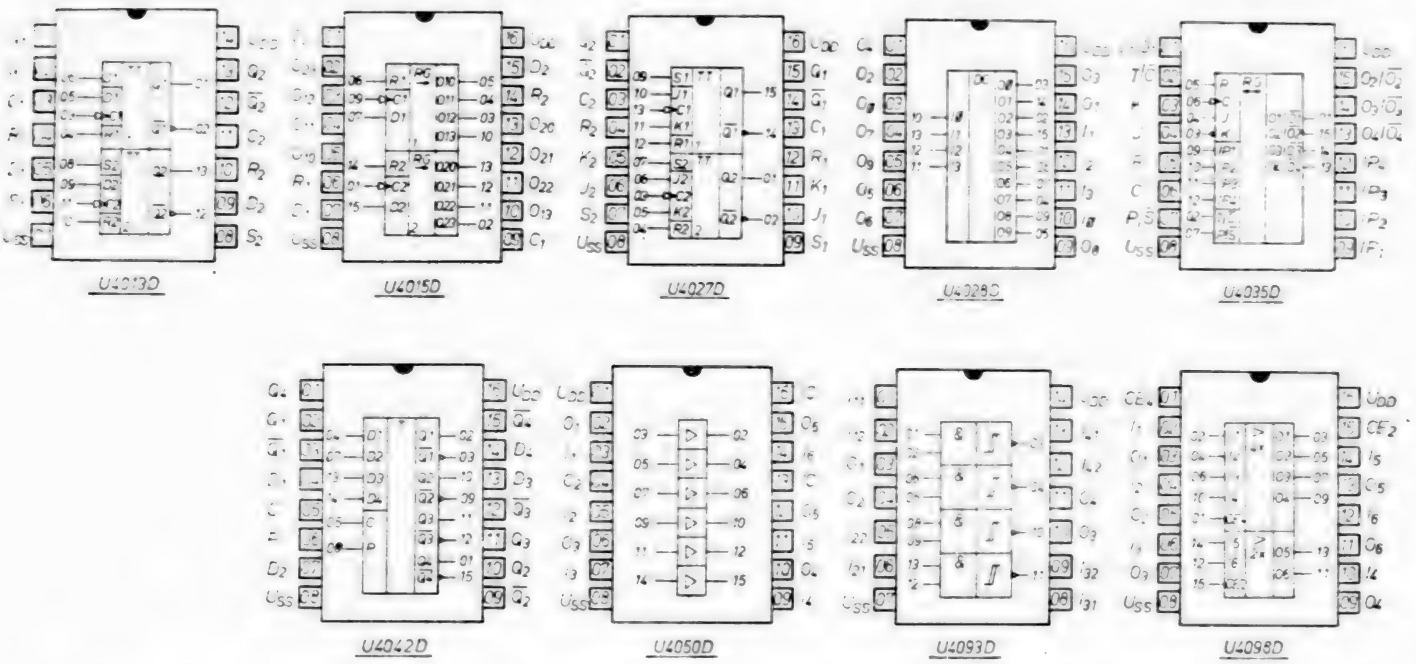


Figure 44. Schematic diagram and wiring of outlets of unipolar CMOS integrated circuits
(last circuit at right bottom is U40098D)

[No 12, Dec 1983 pp 455-498]

[Excerpt] [Part 11] Optoelectronic Coupling Elements RFT

The optoelectronic coupling elements RFT produced by the TV Electronics Plant [Werk fuer Fernsehelektronik] in Berlin use infrared diodes as a source of infrared radiation that are excited by analog or digital signals. Opposite the radiation source in a common casing is located a receiver sensitive to light. The casing protects the optoelectronic system against the effects of external light. At the present time the plant is turning out a total of six types of optoelectronic coupling elements that are virtually unknown in our country.

The type MB101 consisting of an infrared diode and a phototransistor comes in a plastic casing with axial outlets. Its dimensions and the wiring of its outlets are shown in Figure 80. The element serves for galvanic separation of two current circuits with a great difference in potential between the input and output circuits (test voltage of the element is ±5 kV) primarily in control and regulation technology.

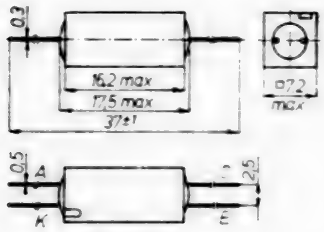


Figure 80. External finish and wiring of outlets of the MB101 optoelectronic coupling element

Elements of the MB104 series--which comes in four groups, A through D, depending on the collector current--are built into a DIL plastic casing with 2x three outlets. The overall power dissipation of an element can be 260 mW, the range of permissible ambient operational temperatures is between -55 to +88°C. Wiring of outlets: 1--anode of infrared (IR) diode; 2--cathode of IR diode; 3--free outlet; 4--phototransistor emitter; 5--phototransistor collector; 6--phototransistor base.

The threshold frequency of optoelectronic coupling elements with output phototransistors in digital transmission is approximately 50 kHz, current amplification factor 1 to 100 percent. Optoelectronic coupling elements with output photodiodes transfer digital signals with a frequency of 1 to 3.5 MHz. Their output current ranges from several μA to 16 mA with a built-in amplifier (in the MB111).

A typical representative of an element with an input IR diode and an output photodiode is the MB110 type. It also comes in a DIL plastic casing with 2x three outlets. It can operate in an ambient temperature range of -25 to +70°C. This element is substantially faster than similar elements with phototransistors. Its average rise and drop time is 50 ns. Wiring of outlets: 1--anode of IR diode; 2--cathode of IR diode; 3--free; 4--anode of photodiode; 5--cathode of photodiode; 6--free.

The MB111 optoelectronic coupling element consists of an input IR diode, with a silicon photodiode on its output with an integrated amplifier connected to the former as a receiver. It also serves for galvanic separation of current circuits with a high difference in potentials, but in essence it represents a certain type of a hybrid logic circuit. It is compatible with TTL integrated circuits and performs the logic function $Y = \bar{A}$ with positive logic. The collector circuit of the output transistor is open.

The MB111 element comes in a DIL plastic casing with 2 x four outlets. Wiring of outlets: 1--anode of IR diode; 2--cathode of IR diode; 3, 4--free; 5--output Y of integrated amplifer; 6--grounding point of integrated

amplifier; 7--supply voltage U_{CC} of integrated amplifier; 8--internal connection of integrated amplifier. Electric values of the element are shown in Tables 46 and 47. The element is designed to operate in a temperature range of -25 to +70°C. The power dissipation P_{tot}, listed in Table 46, is given by the relation $P_{tot} = U_{CC} \cdot I_{SL} + U_{OL} \cdot I_{OL}$.

Table 46. Electric values of RFT optoelectronic coupling elements

Type	Input diode		Output transistor diode*		Characteristic data			Input/output circuit				
	U_R max. [V]	I_F max. [mA]	U_{CB} max. [V]	P_{tot} max. [mW]	I_C pH I_R* [mA	U_{CE} U_R* [V]	I_F [mA]	U_{IO} [kV]	R_{IO} [Ω]	C_{IO} [pF]	K_{IO} min [%]	t_r t_f [μs]
MB101	2	50	15	50	0,0001	15	0	5	10^{12}	0,35	4	5
					1,5	5	35					
MB104A	6	40	32	200	>4	5	10	4,3	$>10^{11}$		40	2 ≤10
MB104B	6	40	32	200	10—28	5	10	4,3	$>10^{11}$		100	2 ≤10
MB104C	6	40	32	200	>16	5	10	4,3	$>10^{11}$		160	2 ≤10
MB104D	6	40	32	200	24—48	5	10	4,3	$>10^{11}$		240	2 ≤10
MB110	3	100	50*		<0,0005*	20*	0	2,8	$>10^{11}$	1	0,2	0,05 <0,25
					<0,01*	50*	0					
					>0,075*	20*	50					
MB111	3	30	7	150				2,8	$>10^{11}$			0,1
MB123	2	50	15	100	<0,0005	5	0				>4	5 <25
					<0,01	15	0					
				typ A:	>0,4	5	15					
				typ B:	>1,0	5	15					
MB125	3	50	16		1,5 >0,4	5	10				>4	10

Another MB123 optoelectronic coupling element consists of a galium arsenide IR diode as transmitter and a silicon phototransistor as receiver. However, it is of open structure with a 3.2--mm air gap between transmitter and receiver. It can be used as an optoelectronic switch (contactless switch, miniature light gate, etc.), in which coupling between input and output is affected from the outside. To guarantee reliable functioning, the element must be screened from outside illumination. The external finishing of the MB123 element is shown in Figure 81. Key electric values are shown in Table 46. The forward d.c. voltage of the input diode at current of 35 mA is on the average 1.25 V, max. 1.9 V. Range of permissible ambient temperatures -25 to + 70°C.

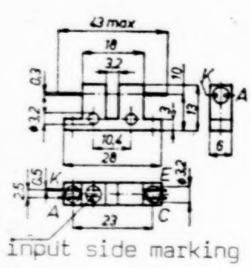


Figure 81. External finish and wiring of outlets of the MB123 optoelectronic coupling element

Markings of outlets: K--cathode, A--anode of IR diode; E--emitter; C--collector of phototransistor. The diode side is marked by a circular depression in the casing

Table 47. Electric values of the MB111 optoelectronic coupling element

Operational conditions apply at $-25\ ^\circ C \le \vartheta_a \le +70\ ^\circ C$		nomin.	min.—max.	
Coupling element:				
Recommended feed voltage	U_{CC}	5,0	4,75 až 5,75	V
Input loading factor	N_O		≤ 10	
Insulation resistance				
$U_{IO} = 500$ V	R_{IO}	10^{12}	$\ge 10^{11}$	Ω
Input current - output at level L				
$U_{CC} = 5{,}25$ V, $I_{oL} = 16$ mA	I_{IH}		≤ 15	mA
Input current - output at level H				
$U_{CC} = 4{,}75$ V	I_{IL}		≤ 2	mA
Switching times				
V, $\vartheta_a = 25\ ^\circ C$, $R_L = 400\ \Omega$,				
$C_L = 25$ pF, $I_P = 15$ mA				
delay at switch on	t_{DHL}	0,3		µs
delay at switch off	t_{DLH}	0,5		µs
drop time	t_{THL}	0,1		µs
Input diode:				
Forward d.c.-current				
$I_F = 2{,}5$ mA	U_F	1,1	$\ge 1{,}0$	V
$I_F = 15$ mA	U_F	1,2	$\le 1{,}35$	V
$I_F = 30$ mA	U_F	1,3	$\le 1{,}5$	V
cut-off d.c. voltage				
$U_R = 3$ V	I_R	0,1	≤ 10	µA
Output amplifier:				
Recommended feed voltage	U_{CC}		$\le 7{,}0$	V
Output d.c. current	I_{OL}		≤ 16	mA
Collector d.c. voltage	U_{OH}		≤ 15	V
Output d.c. voltage - level L				
$U_{CC} = 4{,}75$ V, $I_{OL} = 16$ mA, $I_F = 15$ mA	U_{OL}	0,2	$\le 0{,}4$	V
Output collector current - level H				
$U_{CC} = 5{,}25$ V, $I_F = 1$ mA, $U_{OH} = 12$ V	I_{OH}	0,1	≤ 50	µA
$U_{CC} = 5{,}25$ V, $I_F = 0$ mA, $U_{OH} = 15$ V	I_{OH}	0,1	≤ 200	µA
Power input - output at level L				
$U_{CC} = 5{,}25$ V, $I_F = 30$ mA	I_{SL}	12	≤ 25	mA
Power input - output at level H				
$U_{CC} = 5{,}25$ V, $I_F = 0$ mA	I_{SH}	6	≤ 15	mA

Also under development is the MV125 miniature optoelectronic coupling element of the reflexive type. It comes in a plastic casing in which a receiver and a transmitter are built in independently. Its external finish is shown in Figure 82. The forward voltage of the input diode at a current of 50 mA is on the average 1.3 V, max. 1.6 V. The average rise and drop time of the element is 10 µs at feed voltage of 15 V, collector current of 150 µA and load resistance of 1 kΩ. The average value of collector current of 1.5 mA, min. 0.4 mA applies at diode current of 10 mA, collector feed voltage of 5 V during interception of a light beam reflected from a polished aluminum surface at a distance of 1.5 mm from the upper edge of the diode lens to the aluminum plate. Crosstalk (the ratio of collector current during radiation into free space to collector current during reflection) is put by the manufacturer at an average of 2.5 percent, max. 8 percent at diode current of 10 mA and collector voltage of 5 V. The element must be screened against foreign radiation to ensure proper functioning. The permissible range of ambient operational temperatures is -25 to +85°C. Table 48 shows similar types of optoelectronic elements with comparable properties turned out by some top world producers in comparison with RFT products.

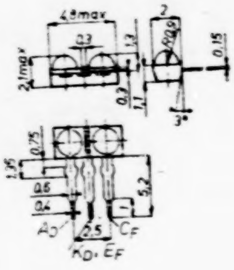


Figure 82. External finish and wiring of outlets of the MB125 optoelectronic coupling element
Outlet markings: A_D--anode of IR diode; K_D--cathode of IR diode; E_F--emitter of phototransistor (common outlet); C_F--collector of phototransistor

Table 48. Table comparing RFT optoelectronic coupling elements

RFT	Siemens	General Instruments Monsanto	Telefunken	Texas Instruments	Valvo
MB101	—	MCT5—10	(CNY21)	TIL109	(CNY42)
MB104	(CNY17)	MCT210	(CQY80)	TIL124, TIL125, TIL125	—
MB110	—	MCD2	—	—	—
MB111	—	MCL611	—	—	—
MB125	—	SFH900	—	—	—

(Types shown in brackets are only approximately comparable.)

8204
CSO: 8112/1034 END

END OF
FICHE
DATE FILMED

7 JUNE 1984